3CH PMU with HV Buck, Boost, Super Capacitor Charger

Features

- 3CH: Buck, Boost and Super Capacitor Charger
- CH1 Buck: Standoff 50V, V_{IN} 7.5-42V, V_{OUT}=3.3V, 1A, 700kHz, PFM Mode for High Efficiency in Light Load
- CH2 Boost: V_{IN} 0.4V-2.55V/V_{OUT} V_{IN}-18V, 1MHz, V_{FB}0.8V
- CH3 Super Capacitor Charger: ±2% accuracy for Charger CV Voltage, 50mA Constant Charge Current
- Enable Pin to auto-switch Boost and Charger
- Over Current Protection
- Over Voltage Protection
- Short Protection with Foldback-Mode
- Thermal Shutdown
- Available in ESOP8, DFN8-3×3 and DFN10-3×3 Packages
- -40°C to +85°C Temperature Range

Applications

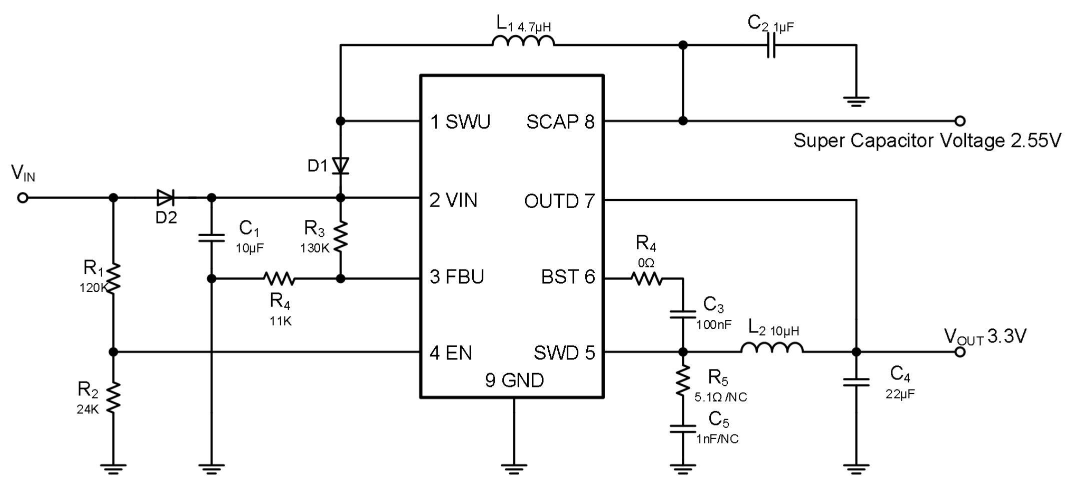
- PLC Modules
- Power Meters

General Description

The GP1301 is a 3-channel PMU that includes a 7.5-42V input, high efficiency synchronous buck converter, a low startup, high efficiency 18V boost converter and a supercapacitor charger. The input voltage of buck converter is up to 42V and deliver a 3.3V output with up to 1A current. A linear supercapacitor charger is also integrated with a very high accuracy CV voltage. The output voltage of boost can be adjusted by external resistor divider.

The GP1301 requires a minimal number of readily available, external components and is available in ESOP8, DFN8-3×3 and DFN10-3×3 packages.

Typical Application Circuit



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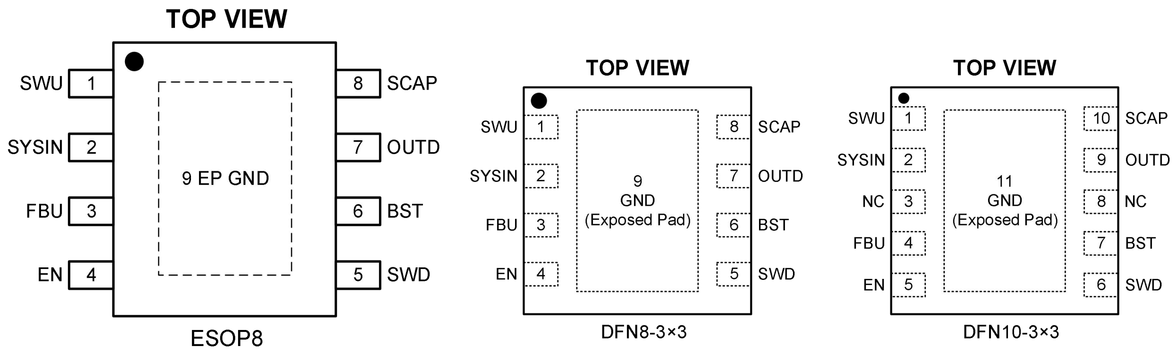
Basic Application Circuit

Pin Description

Pin Configuration



Top Marking:

hzYLL (device code: hz, Y=year code, LL= lot number code, ESOP8)

HYYLL (device code: HY, Y=year code, LL= lot number code, DFN8-3×3)

hvYLL (device code: hv, Y=year code, LL= lot number code, DFN10-3×3)

Pin Description

ESOP8 Pin No.	DFN8-3×3 Pin No.	DFN10-3×3 Pin No.	Name	Function
1	1	1	SWU	Switch Pin for BOOST.
2	2	2	SYSIN	System Power Supply Pin.
-	-	3/8	NC	Not Connected.
3	3	4	FBU	Feedback Pin for BOOST. Connects FBU to the center point of the external resistor R3 and R4.
4	4	5	EN	Enable Pin for auto-switching BOOST and CHARGER EN=0, BOOST is on, CHARGER is off EN=1, BOOST is off, CHARGER is on
5	5	6	SWD	Switch Pin for BUCK.
6	6	7	BST	Bootstrap Pin for BUCK. A capacitor connected between SWD and BST pins is required to form a floating supply across the high-side switch driver.
7	7	9	OUTD	Output Voltage Pin for BUCK, it’s internally

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				setting to 3.3V. It's also the input of CHARGER
8	8	10	SCAP	SUPER CAPACITOR output. It's internally programed to CV at 2.55V
9	9	11	GND	Exposed Pad, it must be connected to Ground.

Order Information

Marking	Part No.	Model	Description	Package	T/R Qty
hzYLL	TBD	GP1301AP8	GP1301AP8 3CH PMU, 42V Buck with 50V standoff, 18V Boost, Supercapacitor Charger, ESOP8	ESOP8	3000pcs
HYYLL	TBD	GP1301AD8	GP1301AD8 3CH PMU, 42V Buck with 50V standoff, 18V Boost, Supercapacitor Charger, DFN8-3×3	DFN8-3×3	3000pcs
hvYLL	TBD	GP1301AD10	GP1301AD10 3CH PMU, 42V Buck with 50V standoff, 18V Boost, Supercapacitor Charger, DFN10-3×3	DFN10-3×3	3000pcs

Specifications

Absolute Maximum Ratings (1) (2)

Item	Min	Max	Unit
V_{IN} voltage	-0.3	50	V
SWD, EN voltage	-0.3	50	V
SWU voltage	-0.3	20	V
BST to SWD voltage	-0.3	6	V
All other Pins voltage	–0.3	6	V
Power dissipation (3)	Internally Limited		
Operating junction temperature, T_J	-40	150	°C
Storage temperature, T_{stg}	–55	150	°C
Lead Temperature (Soldering, 10sec.)		260	°C

Note (1): Exceeding these ratings may damage the device.

Note (2): The device is not guaranteed to function outside of its operating conditions.

Note (3): The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, $R_{\theta JA}$, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{D(MAX)} = (T_{J(MAX)} - T_A)/R_{\theta JA}$. Exceeding the maximum allowable power dissipation causes excessive die temperature, and the regulator goes into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=160°C (typical) and disengages at T_J= 130°C (typical).

ESD Ratings

Item	Description	Value	Unit
$V_{(ESD\text{-}HBM)}$	Human Body Model (HBM) ANSI/ESDA/JEDEC JS-001-2014 Classification, Class: 2	±2000	V
$V_{(ESD\text{-}CDM)}$	Charged Device Mode (CDM) ANSI/ESDA/JEDEC JS-002-2014 Classification, Class: C0b	±500	V
$I_{LATCH\text{-}UP}$	JEDEC STANDARD NO.78E APRIL 2016 Temperature Classification, Class: I	±150	mA

Recommended Operating Conditions

Item	Min	Max	Unit
Operating junction temperature (1)	–40	125	°C
Operating temperature range	-40	85	°C
SYSTEM Input voltage V_{IN}	7.5	42	V
BUCK Output current	0	1	A

Note (1): All limits specified at room temperature (T_A = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Thermal Information (1)(2)

Item	Description	DFN8-3 ×	DFN10-3	ESOP8	Unit

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		3	×3		
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1)(2)	40.2	40.6	48.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	49.7	45.5	52.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.7	15.9	25.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	0.4	8.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.9	15.7	25.2	°C/W
$R_{\theta JC}$	Junction-to-case (Bottom) thermal resistance	4.1	2.8	6.5	°C/W

Note (1): The package thermal impedance is calculated in accordance to JESD 51-7.

Note (2): Thermal Resistances were simulated on a 4-layer, JEDEC board.

Electrical Characteristics (1) (2)

V_{IN}=12V, T_A=25°C, unless otherwise specified.

Parameter	Test Conditions	Min	Typ.	Max	Unit
BUCK					
BUCK Input Standoff Voltage			55		V
BUCK Input Voltage Range		7.5		42	V
BUCK Input OVP	Rising, Hysteresis=1V		43		V
Supply Current (Quiescent)	V_{EN} =3.0V, V_{FB}=1.1V		0.6	0.8	mA
Supply Current (Shutdown)	V_{EN} =0 or EN = GND			4	uA
VOUD Voltage	Internally Setting	3.230	3.300	3.370	V
High-Side Switch On-Resistance	I_{SWD}=100mA		500		mΩ
Low-Side Switch On-Resistance	I_{SWD}=100mA		300		mΩ
High-Side Switch Leakage Current	V_{EN}=0V, V_{SWD}=0V		0	1	μA
Upper Switch Current Limit	Minimum Duty Cycle	1.4			A
Low-Side Zero Crossing Limit			20		mA
Oscillation Frequency			700		KHz
Minimum On-Time			90		nS
Under-Voltage Lockout Threshold	Wake up V_{IN} Voltage		7.5		V
	Shutdown V_{IN} Voltage		4.5		V
	Hysteresis V_{IN} voltage		3		V
BOOST					

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BOOST Input Range		0.7		6	V
FBU Feedback Voltage			800		mV
FBU Input Current	FBU=0 and 2V			1	μA
BOOST Output Voltage Range		5		18	V
BOOST Switching Frequency			1		MHz
Maximum Duty Cycle		95			%
NMOS Switch On Resistor	I_{SWU}=100mA		55		mΩ
NMOS Switch Current Limit				3.5	A
SWU Leakage Current	V_{EN}=0V, V_{SWU}=0V			10	μA
CHARGER					
CV Voltage		2.5	2.55	2.6	V
Charge Current			50		mA
Dropout Voltage	I_{OUT}=30mA		70		mV
Reverse Leakage Current	SCAP=3.5V, OUTD=3.3V			30	μA
SYSTEM					
Quiescent Current	FBU=0.9V, OUTD=3.6V		0.7		mA
EN Input Current			0		μA
EN Rising Threshold			1.50		V
EN Falling Threshold			1.34		V
EN Hysteresis			0.16		V
Soft Start			300		μS
Thermal Shutdown			150		℃
Thermal Hysteresis			30		℃

Note (1): MOSFET on-resistance specifications are guaranteed by correlation to wafer level measurements.

Note (2): Thermal shutdown specifications are guaranteed by correlation to the design and characteristics analysis.

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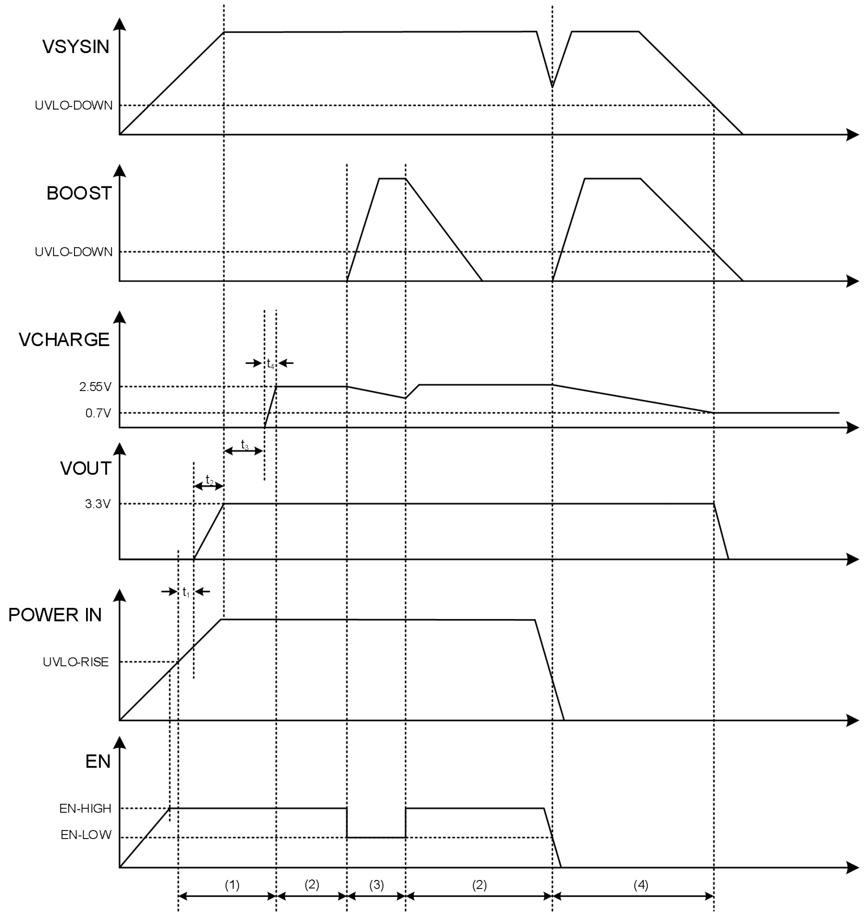
Timing Chart



Remark:

t_1: BUCK start delay time is about 200μs. t_2: BUCK rise time is about 300μs.

t_3: V_C start delay time is about 3ms. t_4: V_C rise time is related to super capacitor capacitance and charging current.

(1) Startup state. (2) Normal state. (3) EN controls super capacitor charging and discharging.

(4) Input power down, super capacitor discharge.

Note: The length of the line in the timing diagram has nothing to do with the actual ratio, only for schematic reference.

When the external input reaches the UVLO-RISE of CH1, 3.3V starts to rise after the delay time of t_1. When the 3.3V rise is completed, then after the delay time of t_3, CH3 starts to start. EN can follow the external input (affected by the ratio of R_1 and R_2), or it can add a control signal to control the charging and discharging of the super capacitor.

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Functions Description

The GP1301 is a 3-channel PMU that includes a wide input, high efficiency synchronous buck converter, a low startup, high efficiency boost converter and a supercapacitor charger. The buck converter and withstand input voltage up to 42V and deliver a 3.3V output with 1A continuous current. The boost converter is capable of providing up to 350mA to 12V output from a single cell supercapacitor or a battery at 2.55V. A linear supercapacitor charger is also integrated with a very high accuracy CV voltage. The output voltage of boost can be adjusted by external resistor divider.

Buck converter

The BUCK is a wide input range, high-efficiency, synchronous step-down switching regulator which output is fixed at 3.3V, capable of delivering up to 1A of output current. With a fixed switching frequency of 700KHz, this current mode PWM controlled converter allows the use of small external components, such as ceramic input and output caps, as well as small inductors. It also employs a proprietary control scheme that switches the device into a power save mode during light load, thereby extending the range of high efficiency operation. An OVP function protects the IC itself and its downstream system against input voltage surges. With this OVP function, the IC can stand off input voltage as high as 50V.

Boost converter

The BOOST is a high efficiency no-synchronous step up converter. It can deliver at least 4.2W of power from 2.55V, 0.35A at 12V output. A switching frequency of 1MHz solution footprint by allowing the use of tiny and low-profile inductors and ceramic capacitors. The output of BOOST can be set by external resistor divider at FBU pin.

CHARGER

The CHARGER is fully integrated constant current (CC)/constant voltage (CV) function. It can deliver a 50mA charge current with a final float voltage of 2%. It also integrated reverse protection, when OUTD is low than SCAP to protect the Supercapacitor not to discharge.

Enable

EN is a digital control pin that turns the BOOST and CHARGER on and off, Drive EN High to turn on the CHARGER and turn off the BOOST, drive it Low to turn off the CHARGER and turn on the BOOST.

Over-Temperature Protection

Thermal protection disables BUCK, BOOST and CHARGER when the junction temperature rises to approximately 150℃, allowing the device to cool down. When the junction temperature cools to approximately 130℃, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits regulator dissipation, protecting the device from damage as a result of overheating.

Under-Voltage Lockout (UVLO)

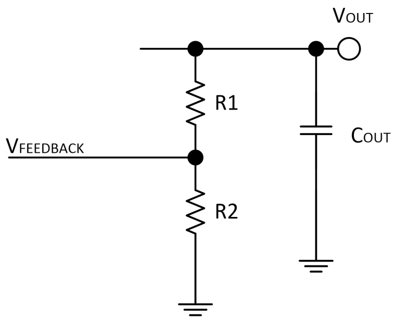
Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. When the voltage is higher than UVLO threshold voltage, the device is enabled again.

Applications Information

Setting the BOOST Output Voltage

GP1301 require an input capacitor, an output capacitor and an inductor. These components are critical to the performance of the device.GP1301 are internally compensated and do not require external components to achieve stable operation. The output voltage can be programmed by resistor divider.

$$V_{OUT} = V_{FB} \times \frac{R1 + R2}{R2}$$



BOOST On/Off and Super capacitor charge and discharge vs. En threshold

The GP1301 EN pin also servs as a threshold voltage for auto-switching Supercapacitor Charger and the BOOST. When the VIN drops, and EN's voltage is below the falling threshold ($V_{EN\_FALLING}$ = 1.34V), the Supercapacitor Charger is disabled and the BOOST is then enabled at the same time. With a resistor ladder, R1 from VIN to EN and R2 from EN to GND, the VIN dropping threshold thus is programmed by the equation below.

$$V_{IN\,Threshold} = V_{EN\_FALLING} \times \left(1 + \frac{R_1}{R_2}\right)$$

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Selecting the Inductor for BUCK

The recommended inductor values are shown in the application diagram. It is important to guarantee the inductor core does not saturate during any foreseeable operational situation. The inductor should be rated to handle the peak load current plus the ripple current: Care should be taken when reviewing the different saturation current ratings that are specified by different manufacturers. Saturation current ratings are typically specified at 25°C, so ratings at maximum ambient temperature of the application should be requested from the manufacturer.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times F_{OSC}}$$

Where ΔIL is the inductor ripple current. Choose inductor ripple current to be approximately 30% if the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

Selecting the Inductor for BOOST

The boost converter can utilize small surface mount and chip inductors due to the fast 1MHz switching frequency. Inductor values between 2.2µH and 10µH are suitable for most applications. Larger values of inductance will allow slightly greater output current capability by reducing the inductor ripple current. Increasing the inductance above 10µH will increase size while providing little improvement in output current capability. The minimum boost inductance value is given by:

$$L > \frac{V_{IN} \times (V_{OUT} + V_{DIODE} - V_{IN})}{F_S \times I_{RIPPLE} \times (V_{OUT} + V_{DIODE})}$$

Where

- I_{RIPPLE} : Peak-to-Peak inductor current
- V_{IN} : Input voltage
- V_{OUT} : Output voltage
- V_{DIODE} : Output diode Forward Voltage
- F_S : Switching frequency, Hertz

The inductor current ripple is typically set for 20% to 40% of the maximum inductor current. High frequency ferrite core inductor materials reduce frequency dependent power losses compared to cheaper powdered iron types, improving efficiency. The inductor should have low DCR(series resistance of the winding) to reduce the I2R power losses, and must not saturate at peak inductor current levels. Molded chokes and some chip inductors usually.

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Selecting the Output Capacitor

Special attention should be paid when selecting these components. The DC bias of these capacitors can result in a capacitance value that falls below the minimum value given in the recommended capacitor specifications table.

The ceramic capacitor's actual capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of −55°C to +125°C, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of −55°C to +85°C. Many large value ceramic capacitors, larger than 1uF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25°C to 85°C. Therefore, X5R or X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25°C.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 22uF to 44uF range. Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25°C down to −40°C, so some guard band must be allowed.

PCB Layout Guide

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines for reference.

1. Keep the path of switching current short and minimize the loop area formed by Input capacitor, high-side MOSFET and low-side MOSFET.
2. Bypass ceramic capacitors are suggested to be put close to the VIN Pin.
3. Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
4. VOUT, SW away from sensitive analog areas such as FB.

Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

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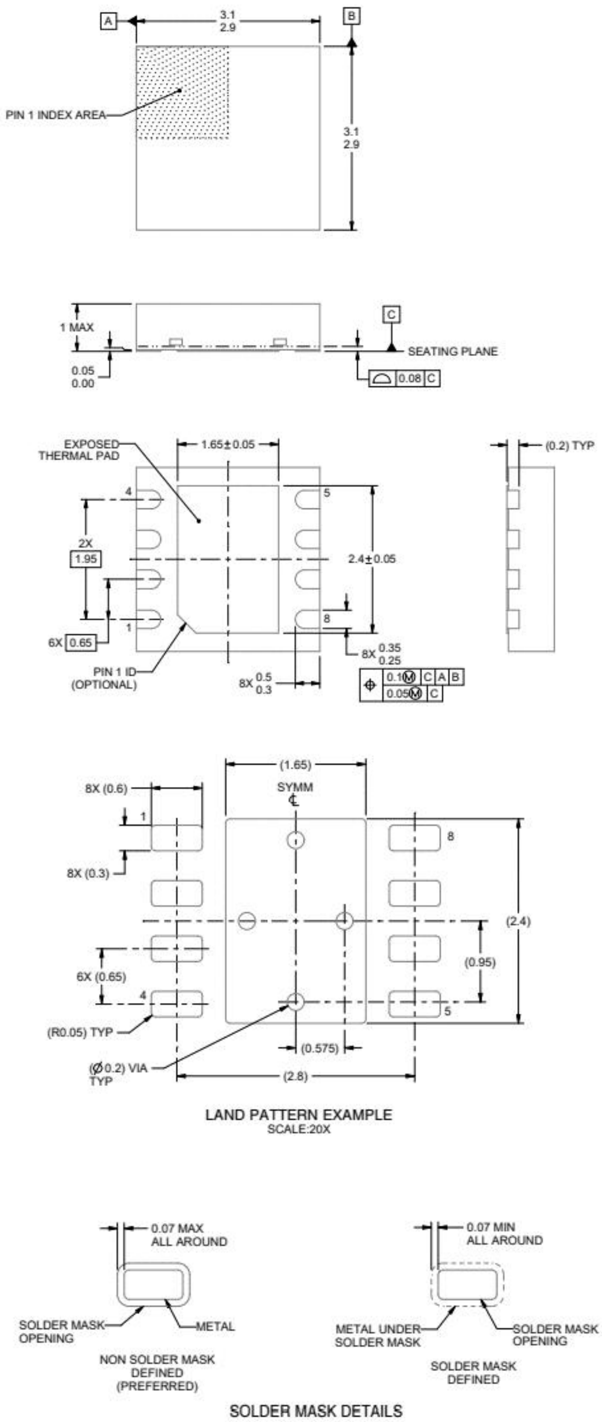
Package Description

8-Pin DFN3×3 Packaging Information



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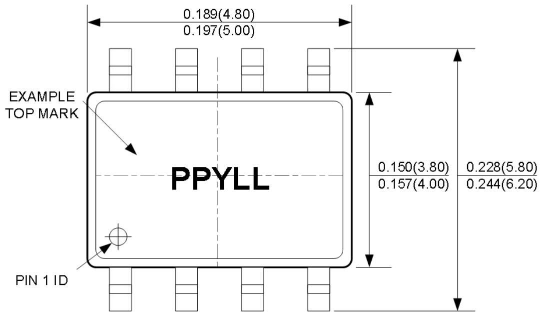
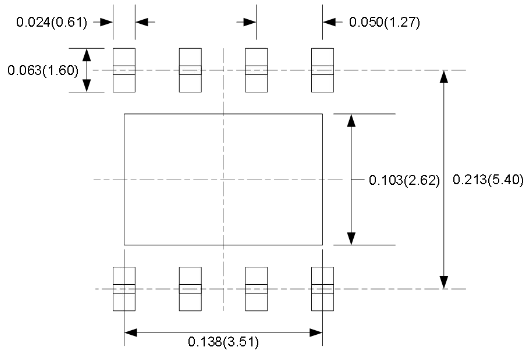
8-Pin ESOP Packaging Information

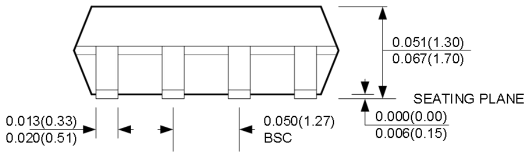
ESOP8 (EXPOSED PAD)



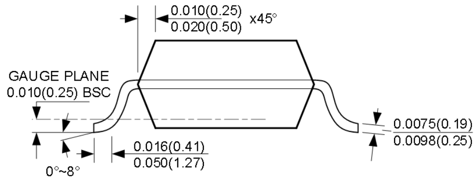
TOP VIEW



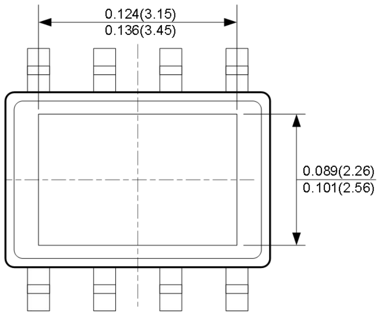
RECOMMENDED PAD LAYOUT



FRONT VIEW



SIDE VIEW



BOTTOM VIEW

NOTE:
1. CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5. DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6. DRAWING IS NOT TO SCALE.

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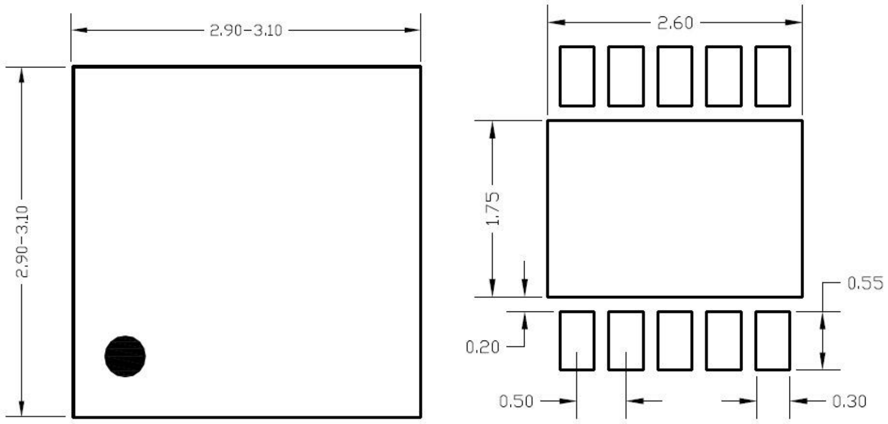
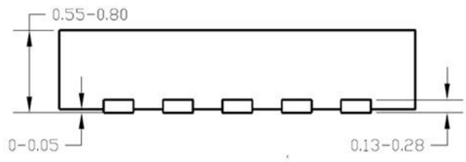
10-Pin DFN3×3 Packaging Information

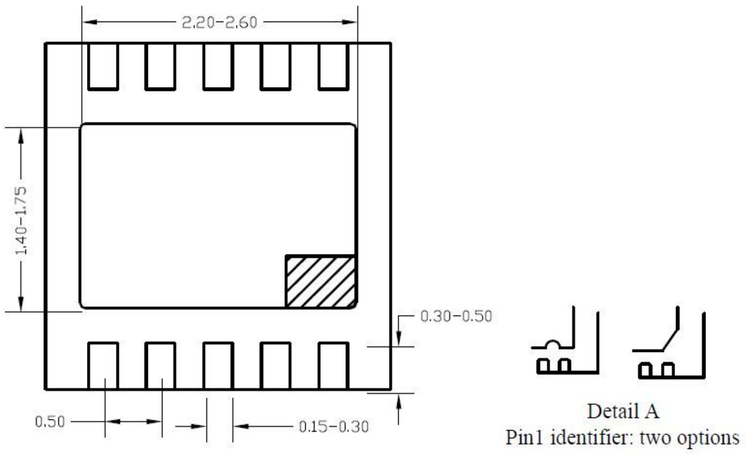
DFN3*3-10



TOP VIEW **RECOMMENDED PAD LAYOUT**



SIDE VIEW



BOTTOM VIEW

NOTE:
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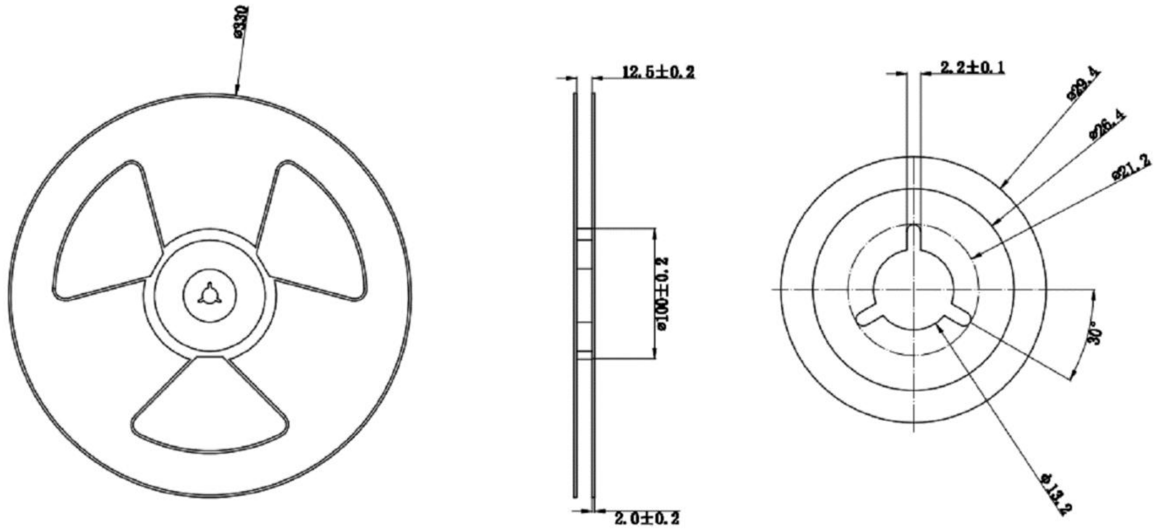
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5. DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6. DRAWING IS NOT TO SCALE.

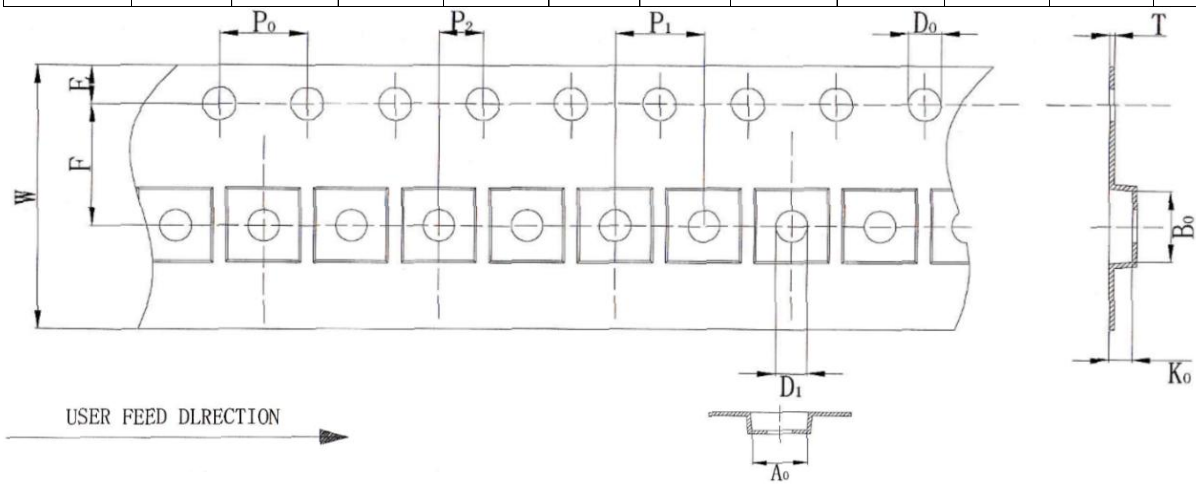
Tape and Reel Information

8-Pin/10-Pin DFN3×3 Tape and Reel Information



Specification	Appropriate Types	Unit
13*12	DFN 3*3	mm

ITEM(mm)	W(mm)	Ao(mm)	Bo(mm)	Ko(mm)	E(mm)	F(mm)	D1(mm)	Do(mm)	Po(mm)	P1(mm)	P2(mm)	t(mm)
MIN	11.70	3.13	3.13	0.95	1.65	5.45	---	---	3.90	3.90	1.95	0.18
NOM	12.00	3.23	3.23	1.05	1.75	5.50	1.50	1.50	4.00	4.00	2.00	0.23
MAX	12.30	3.33	3.33	1.15	1.85	5.55	1.60	1.60	4.10	4.10	2.05	0.28



Note: (1) The cumulative error of any ten gears does not exceed ±0.2mm. (2) Material thickness is subject to carrier tape edge measurement. (3) Straight line bending within 250mm of any length of carrier tape should be less than 1mm. (4) If not specified, the tolerance range: ±0.1mm. (5) Ao, Bo is the depth dimension of the innermost bottom of the cavity. (6) Where the appearance of the cavity

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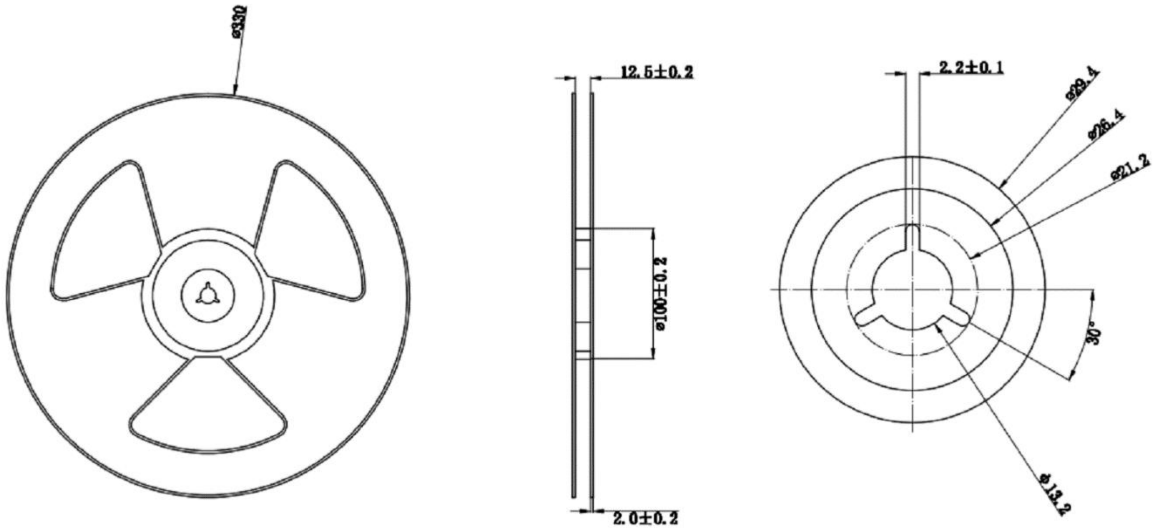
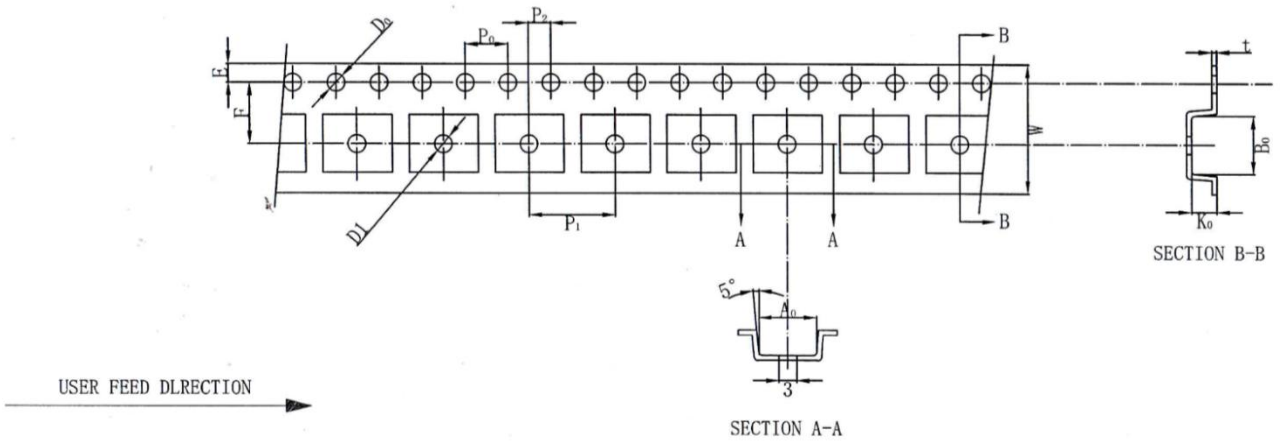
is not marked, the chamfer R is 0.2-0.3mm.

8-Pin ESOP Tape and Reel Information



Specification	Appropriate Types	Unit
13*12	SOP8	mm

ITEM(mm)	W(mm)	Ao(mm)	Bo(mm)	Ko(mm)	E(mm)	F(mm)	D1(mm)	Do(mm)	Po(mm)	P1(mm)	P2(mm)	t(mm)
MIN	11.90	6.50	5.20	1.91	1.65	5.45	---	---	3.90	7.90	1.95	0.185
NOM	12.00	6.60	5.40	2.01	1.75	5.50	1.50	1.50	4.00	8.00	2.00	0.235
MAX	12.10	6.75	5.45	2.11	1.85	5.55	1.60	1.60	4.10	8.10	2.05	0.285



Note: (1) The cumulative error of any ten gears does not exceed ±0.2mm. (2) Material thickness is subject to carrier tape edge measurement. (3) Straight line bending within 250mm of any length of carrier tape should be less than 1mm. (4) If not specified, the tolerance range: ±0.1mm. (5) Ao, Bo is the depth dimension of the innermost bottom of the cavity. (6) Where the appearance of the cavity is not marked, the chamfer R is 0.2-0.3mm.

3CH PMU with HV Buck, Boost, Super Capacitor Charger

Soldering Parameters

Reflow Condition		Pb-Free assembly
Pre Heat	- Temperature Min ($T_{s(min)}$)	+150°C
	- Temperature Max ($T_{s(max)}$)	+200°C
	- Time (Min to Max) (t_s)	60-180 secs.
Average ramp up rate (Liquidus Temp (T_L) to peak)		3°C/sec. Max.
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/sec. Max.
Reflow	- Temperature (T_L) (Liquidus)	+217°C
	- Temperature (t_L)	60-150 secs.
Peak Temp (T_P)		+260(+0/-5)°C
Time within 5°C of actual Peak Temp (tp)		30 secs. Max.
Ramp-down Rate		6°C/sec. Max.
Time 25°C to Peak Temp (T_P)		8 min. Max.
Do not exceed		+260°C