Alveo Debug Kit

User Guide

UG1538 (v1.3) September 29, 2023

AMD Adaptive Computing is creating an environment where employees, customers, and partners feel welcome and included. To that end, we're removing non-inclusive language from our products and related collateral. We've launched an internal initiative to remove language that could exclude people or reinforce historical biases, including terms embedded in our software and IPs. You may still find examples of non-inclusive language in our older products as we work to make these changes and align with evolving industry standards. Follow this link for more information.

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Introduction

The AMD Alveo™ debug kit (ADK2) is the next generation card maintenance and debugging kit, superseding the original Alveo programming cable (aka DMB1). Consisting of a debug module, USB cable, and flexible ribbon cable, it provides communication between a host computer or off-the-shelf debugger and a card with an ADK2 maintenance connector. Improved capabilities include:

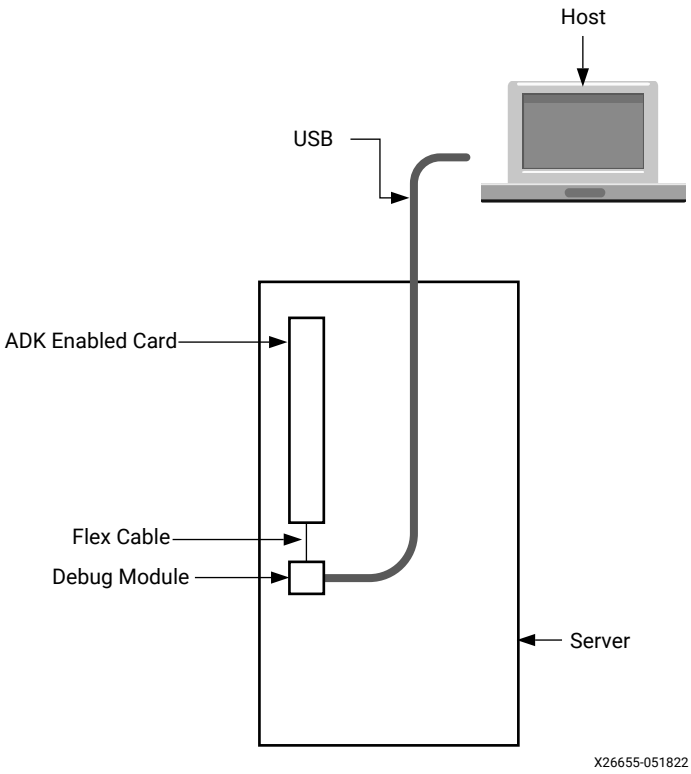
- Boundary scan tests to simplify Alveo card manufacturing
- Application development for SMBus and Arm® subsystem monitoring and debug

In addition, the ADK2 has card customizable support for up to:

- 3 JTAG interfaces
- 4 UARTs
- GPIO and Analog test points
- Third party debug tools

The following figure shows the ADK2 connected to a card in a server and connected to a host computer.

Figure 1: **ADK2 Connection Block Diagram**



Additional documentation and tutorials along with a control application, can be found in the ADK lounge. Contact your AMD sales representative to obtain access.

Chapter 2

Overview

Features

Features of the AMD Alveo™ debug kit (ADK2) are listed in the following table.

Table 1: **Key ADK2 Features**

Feature	Summary
AMD Device JTAG	30 MHz over USB
	100 MHz if using SmartLynq header
Support for multiple UARTS	Typical card UARTs include: • Satellite controller (SuC) • FPGA • Auxiliary on-card processor (SoC)
Support for monitoring up to 16 analog signals	Allows monitoring of on-card voltage rails.
Support for up to 16 GPIOs	Allows for card monitoring and control.
Support for third party accessories	Additional functionality can be enabled by parring a supported accessory with debug module headers documented in Chapter 5: Debug Module Connectors.

Notes:

1. Supported features are card specific. Refer to the card specific documentation for more information.

Ordering Information

Table 2: **Alveo Debug Kit and Accessory Part Numbers**

Part Number	Description
HW-ADK-2-0-G	Alveo debug kit

Notes:

1. To purchase the Alveo debug kit, visit the following link: https://www.xilinx.com/products/boards-and-kits/alveo/accessories.html.

Supported Cards

This kit supports ADK2 enabled cards. See specific card documentation to determine if a card is ADK2 enabled. The following figure is an example of the ADK2 debug connector on an enabled card.

Figure 2: **ADK2 Debug Connector**

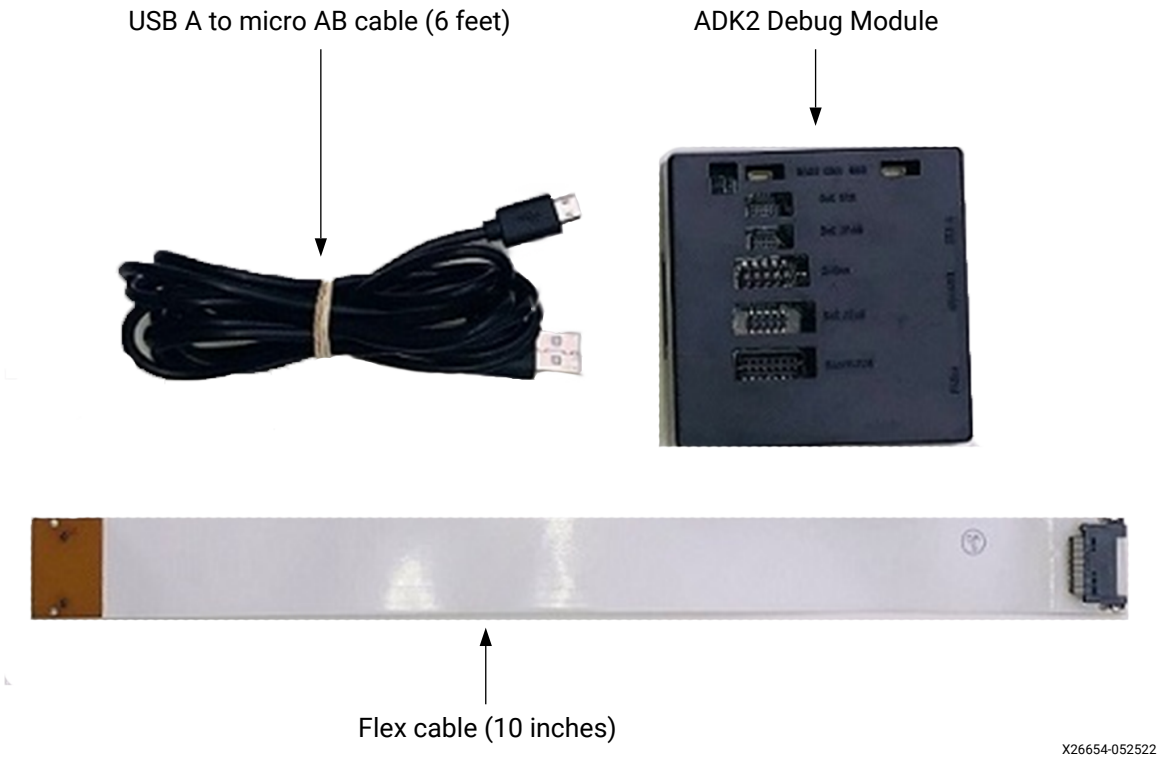
Alveo Debug Kit Contents

The AMD Alveo™ debug kit (ADK2) consists of the following components:

- ADK2 debug module
- 6' USB cable (USB A to micro AB)
- 10" flex cable

The following figure shows the ADK2 components.

Figure 3: **Alveo Debug Kit Content**

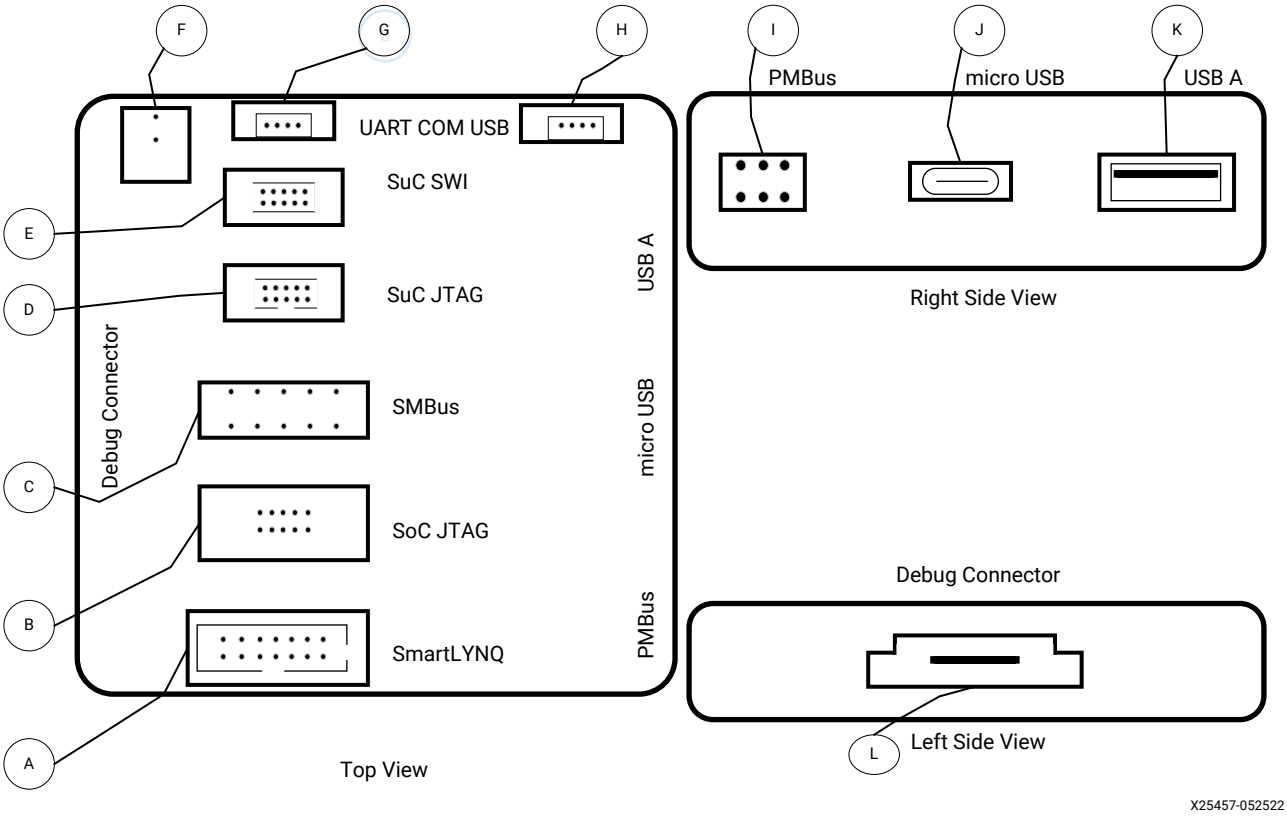


***Note*:** For known issues, see Answer Record 000033996.

Debug Module

The debug module has multiple interfaces, providing access to a host computer and/or other third-party debugger tools. The following figure shows the various interfaces and locations on the debug module.

Figure 4: **ADK2 Debug Module**



***Note*:** Some features are reserved and functionality might change depending on the connected card. See Debug Module and card specific documentation for more information.

The following table describes each connector call-out in Figure 4, listing connector descriptions and links to supported off-the-shelf debuggers (if applicable). Refer to Chapter 5: Debug Module Connectors for pinout descriptions for each connector.

Table 3: **Debug Module Port Description**

Call-out	Interface Name	Connector Description	Compatible External Tool
A	SmartLYNQ	14-pin header Molex 0878321420	AMD SmartLynq Data Cable
B	SoC JTAG	10-pin header Harwin M22-5320505	Arm® SoC JTAG Header, compatible with NXP CodeWarrior

Table 3: **Debug Module Port Description** *(cont'd)*

Call-out	Interface Name	Connector Description	Compatible External Tool
C	SMBus	10-pin header Molex 15-91-0100	Total Phase Aardvark or Beagle I2C Monitor
D	SuC JTAG	10-pin header SAMTEC FTSH-105-01-F-D-K	TI MSP debugger
E	SuC SWI	10-pin header SAMTEC FTSH-105-01-F-D-K	Segger J-link or LPC Link2 debugger
F	Proj	Reserved	Reserved
G	COM UART	4-pin header Amhhenol 10147605-00004LF	Reserved
H	COM USB	4-pin header Amhhenol 10147605-00004LF	Reserved
I	PMBus	6-pin header Amphenol 68021-406HLF	Renesas PMBus Dongle
J	Micro USB	Provides debug module power and host connection. Must be connected.	N/A
K	USB A	USB A connector Wurth 629104190121	Reserved
L	ADK2 Debug Connector	Keyed connection for the flex cable.	N/A

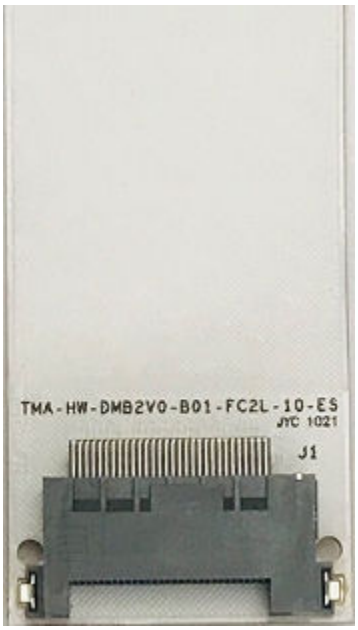
Flex Cable

The 10-inch flex cable provides connection between the debug module and the ADK2 enabled card. The flex cable has been designed for high data rates and durability. To guide a correct connection, each end of the cable has an identical keyed connector with re-enforced stiffeners (see Figure 5).

***Note*:** While the cable can bend up to 180 degrees, with a bending radius of around 15 mm, over-stressing the cable can cause damage.

***Note*:** When disconnecting the cable gently pull out in a straight line.

Figure 5: **Flex Cable Connector**



USB Cable

The debug module is powered through the micro USB interface and provides communication between the debug module and host computer. The ADK2 includes a six foot USB cable to provide access to a debug module placed inside of a server. If this cable is not long enough use a compatible USB cable that fits your needs.

Hardware Setup

This section describes how to setup your debug module for use with a host computer and an ADK2 enabled card. Depending on your system setup, the following installations steps might differ.

Prior to connecting the system, read the Standard ESD Measures.

Standard ESD Measures

CAUTION! *ESD can damage electronic components when they are improperly handled, and can result in total or intermittent failures. Always follow ESD-prevention procedures when removing and replacing components.*

CAUTION! *L'ESD peut endommager les composants électroniques lorsqu'ils sont mal manipulés, et peut entraîner des défaillances totales ou intermittentes. Suivez toujours les procédures de prévention contre les ESD lors du retrait et remplacement des composants.*

CAUTION! *Elektrostatische Entladung (ESD) kann elektronische Bauteile beschädigen, wenn sie unsachgemäß behandelt werden, und es kann zu totalen oder zeitweiligen Ausfällen kommen. Befolgen sie beim Entfernen und Austauschen von Komponenten stets die ESD-Schutzmaßnahmen.*

To prevent ESD damage:

- Attach a wrist strap to an unpainted metal surface of your hardware to prevent electrostatic discharge from damaging your hardware.
- When you are using a wrist strap, follow all electrical safety procedures. A wrist strap is for static control. It does not increase or decrease your risk of receiving electric shock when you are using or working on electrical equipment.
- If you do not have a wrist strap, before you remove the product from ESD packaging and installing or replacing hardware, touch an unpainted metal surface of the system for a minimum of five seconds.
- Do not remove the device from the antistatic bag until you are ready to install the device in the system.
- With the device still in its antistatic bag, touch it to the metal frame of the system.

- Grasp cards and boards by the edges. Avoid touching the components and gold connectors on the adapter.
- If you need to lay the device down while it is out of the antistatic bag, lay it on the antistatic bag. Before you pick it up again, touch the antistatic bag and the metal frame of the system at the same time.
- Handle the devices carefully to prevent permanent damage.

Connecting the Debug Module

This section provides steps for connecting the debug module to the host and the ADK2 enabled card. The following items are required:

- Debug module
- USB cable (USB A to micro AB) long enough for your installation
- Flex cable
- Host computer capable of communicating to the debug module.

  ***Note*:** The debug module is powered from the host computer USB connection. For the debug module to operate the host computer has to be powered on.
- ADK2 enabled card to be installed in a compatible server.

The following flow is recommended for installing and connecting the debug module. These steps might differ depending on your server configuration.

WARNING! *During installation, the server should be powered off and unplugged.*

1. Connect the USB cable to the micro USB port (call-out 10 in Figure 4) of the debug module (shown in Figure 6).

Figure 6: **USB Connected to Debug Module Micro USB Port**

2. Connect the flex cable to the ADK2 debug connector (call-out 12 in Figure 4) on the debug module (shown in Figure 7).

Figure 7: **Flex Cable Connected to Debug Module**

Note: To disconnect the cable gently pull out in a straight line.

3. Power off and unplug the server.
4. Install the ADK2 enabled card in the server leaving the server cover removed.

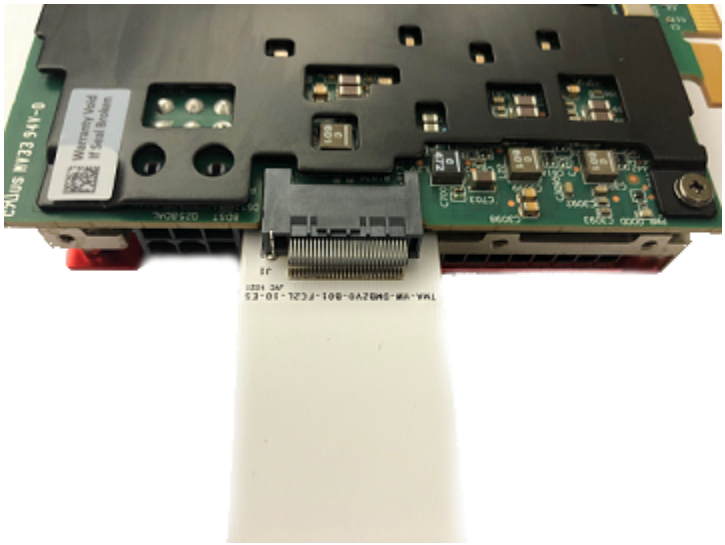
Note: Follow the card installation procedures described in the card specific installation guide.

5. Connect the opposite end of the flex cable to the ADK2 debug connector on the ADK2 enabled card (see Figure 8). Ensure the cable is fully connected. Route the cable on the back side of the card to avoid blocking airflow across the heat sink.

   Note: Alternatively, the flex cable can be hooked to the card before connecting the debug module (see step 2) or installing in the server (see step 4).

   Note: Both the connector and the cable are keyed to help guide a correct connection. Check key orientation when making the connection. To complete the host to debug module connection, it might be necessary to guide the USB cable or the flex cable through an adjacent PCIe® slot.

Figure 8: **Flex Cable Connected to the Card**



   Note: Do not connect or disconnect the flex cable to a card that is powered on. This will cause damage to both the debug module and the card.

6. Replace the server cover.
7. Power on the server.
8. Ensure the host machine is powered on.
9. Connect the opposite end of the USB cable to the host.

The connection between the ADK2 enabled card and the host machine is complete and can be used to program the card via the AMD Vivado™ Hardware Manager. The connection can be tested with AMD Vivado Hardware Manager, the ADK2 control application, or standard OS utilities (i.e., device manager or dmsg). By default, the following features are enabled when the debug module powers up:

- UARTs to connect to the FPGA, SoC, and SuC.
- JTAG enabled through the micro USB.

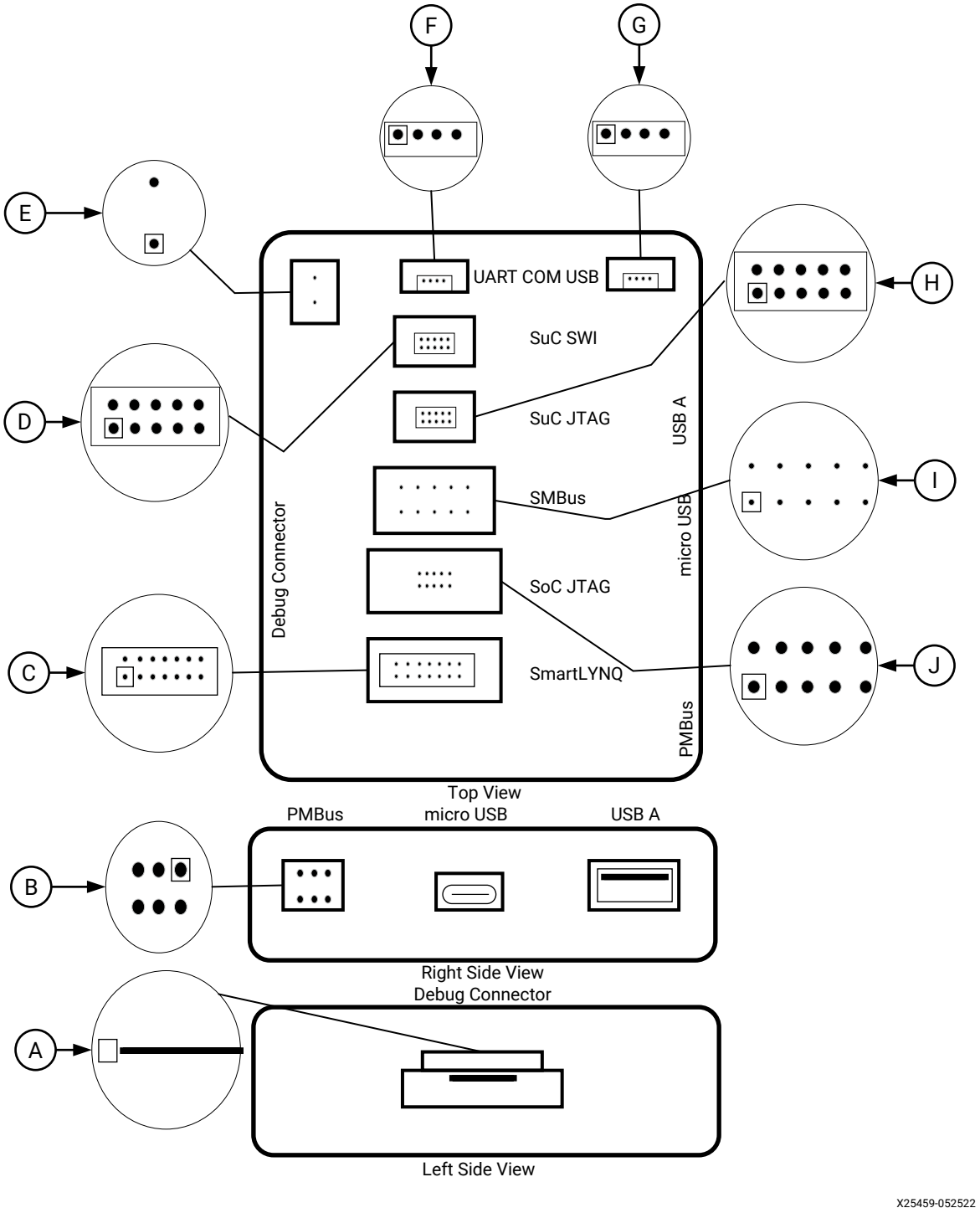
Debug Module Connectors

The following sections provide pin out details for the various connectors on the ADK2 debug module.

Connector Pin Location

Figure 4 has an expanded view of each connector on the debug module with a square around pin 1. The micro USB and USB A connectors match industry standards and are not identified in the following diagram.

Figure 9: **Pin 1 Location**



***Note*:** Pin 1 is not included for USB interfaces. See the standard USB specification for more details.

Debug Connector

The ADK2 debug connector provides support for the following development interfaces:

- AMD device JTAG access
- Multiple UARTs
- Satellite controller JTAG
- PMBus, directly connected to the Renesas dongle header.
- SMBus, directly connected to the Aardvark header for bus monitoring.
- Analog test points for voltage measurement.
- GPIO connections for card monitoring and control.

***Note*:** Not all cards implement all interfaces. See card specific documentation for more details.

The pinout of the flex header is detailed in the following table. The analog test points and GPIOs are defined in card specific documentation.

Table 4: **Flex Header Pinout**

Pin	Signal Name	Pin	Signal Name
A1	SOC_JTAG_VREFIN	B1	FPGA_JTAG_VREFIN
A2	SOC_JTAG_TDI	B2	FPGA_JTAG_TCK
A3	SOC_JTAG_TMS	B3	FPGA_JTAG_TMS
A4	SOC_JTAG_TCK	B4	FPGA_JTAG_TDI
A5	SOC_JTAG_TRST_B	B5	FPGA_JTAG_TDO
A6	SOC_JTAG_TDO	B6	FPGA_SRST_B
A7	SOC_RST_B	B7	SOC_TBSCAN_EN
A8	GND	B8	GND
A9	SOC_UART_VREF	B9	FPGA_UART_VREF
A10	SOC_UART_RXD	B10	FPGA_UART_RXD
A11	SOC_UART_TXD	B11	FPGA_UART_TXD
A12	GND	B12	DEBUG_MODULE_IO_EXP_P13
A13	DUT_PG	B13	SUC_UART_RXD
A14	SUC_JTAG_TCK	B14	SUC_UART_TXD
A15	SUC_JTAG_TRST_B	B15	SUC_SWDIO
A16	SUC_JTAG_TDI	B16	SUC_SWCLK
A17	SUC_JTAG_TMS	B17	SUC_SWO
A18	SUC_JTAG_TDO	B18	SUC_RST_B
A19	DEBUG_MODULE_IO_EXP_P14	B19	DEBUG_MODULE_IO_EXP_P15
A20	ADC1_IN2	B20	SUC_VREFIN

Table 4: **Flex Header Pinout** *(cont'd)*

Pin	Signal Name	Pin	Signal Name
A21	PMBUS_SDA	B21	SMBUS_SDA
A22	PMBUS_SCL	B22	SMBUS_SCL
A23	PMBUS_ALERT_B	B23	SoC_TA_PROG_SFP
A24	GND	B24	GND
A25	ADC1_IN0	B25	ADC1_IN1
A26	ADC0_IN6	B26	ADC0_IN7
A27	ADC0_IN4	B27	ADC0_IN5
A28	ADC0_IN2	B28	ADC0_IN3
A29	ADC0_IN0	B29	ADC0_IN1
A30	DEBUG_MODULE_PRSNT_B	B30	GND

Micro USB Connector

The micro USB connector provides power to the debug module and is the main communication to the host machine. A USB cable must be connected to the micro USB connector to provide power and operate correctly.

Table 5: **Micro USB Connector Pinout**

Pin	Signal	Function
1	USB_VBUS	USB power
2	USB_DN	USB differential pair
3	USB_DP	USB differential pair
4	USB_ID	No Connect
5	GND	Ground

SuC SWI Header

The SuC SWI provides access to the NXP satellite controller when supported by the card. It is compatible with Segger JLINK [Ref 3] or LPC Link2 debuggers [Ref 4]. The header provides the SuC SWDIO voltage reference on the card.

***Note*:** Programming the SuC or SoC firmware/flash using the ADK2 might void warranty and should only be performed by qualified experts or under factory guidance.

Table 6: **SuC SWI Header Pinout**

Signal	Pin	Pin	Signal
SUC_VREF	1	2	ucSWDIO
GND	3	4	ucSWCLK
GND	5	6	ucSWO
NC	7	8	NC
GND	9	10	ucRST

SuC JTAG Header

The SuC JTAG provides access to the TI-MSP satellite controller when supported by the card. It is compatible with TI MSP-FET [Ref 5]. The header provides the SuC JTAG voltage reference (SUC_VREF) on the card.

***Note*:** Programming the SuC or SoC firmware/flash using the ADK2 might void warranty and should only be performed by qualified experts or under factory guidance.

Table 7: **SuC JTAG Header Pinout**

Signal	Pin	Pin	Signal
SUC_VREF	1	2	SUC JTAG TMS
GND	3	4	SUC JTAG TCK
GND	5	6	SUC JTAG TDO
NC	7	8	SUC JTAG TDI
GND	9	10	SUC RST

SoC JTAG Header

The SoC JTAG provides access to the NXP application processor when supported by the card. It is compatible with the NXP CodeWarrior Tap debugger [Ref 8]. It provides the SoC JTAG voltage reference (SoC_VREF) on the card.

Table 8: **SoC JTAG Header Pinout**

Signal	Pin	Pin	Signal
SoC_VREF	1	2	SoC JTAG TMS
GND	3	4	SoC JTAG TCK
GND	5	6	SoC JTAG TDO
NC	7	8	SoC JTAG TDI

Table 8: **SoC JTAG Header Pinout** *(cont'd)*

Signal	Pin	Pin	Signal
GND	9	10	SoC RST

AMD SmartLynq Header

The AMD SmartLynq is compatible with the AMD SmartLynq programming cable [Ref 9]. It provides FPGA JTAG voltage reference (FPGA_JTAG_VREF) on the card.

This header provides JTAG support at 100 MHz. JTAG support is also provided through the micro USB connector, but only at 30 MHz.

Table 9: **AMD SmartLynq Header Pinout**

Signal	Pin	Pin	Signal
NC	1	2	FPGA_JTAG_VREF
GND	3	4	FPGA JTAG TMS
GND	5	6	FPGA JTAG TCK
GND	7	8	FPGA JTAG TDO
GND	9	10	FPGA JTAG TDI
GND	11	12	NC
PGND	13	14	FPGA SRST

SMBus Header

The SMBus provides access to the card's SMBus interface when supported by the card. It is compatible with the Total Phase Aardvark host adapter [Ref 6] or Total Phase Beagle I2C Monitor protocol analyzer [Ref 7].

***Note*:** When using an external tool, exercising SMBus master function can overlap with server BMC access and can hang the bus.

Table 10: **SMBus Header Pinout**

Signal	Pin	Pin	Signal
SMBUS_SCL	1	2	GND
SMBUS_SDA	3	4	NC
NC	5	6	NC
NC	7	8	NC

Table 10: **SMBus Header Pinout** *(cont'd)*

Signal	Pin	Pin	Signal
NC	9	10	GND

PMBus Header

The PMBus header provides access to the card's PMBus interface when supported by the card. It is compatible with the Renesas PMBus dongle [Ref 10].

***Note*:** When using an external tool, the satellite controller must be in reset, otherwise accesses from the external tool and satellite controller will overlap and hang the bus.

Table 11: **PMBus Header Pinout**

Signal	Pin	Pin	Signal
NC	1	2	NC
GND	3	4	PMBUS_SCL
PMBUS_ALERTB	5	6	PMBUS_SDA

Analog Test Points

The debug module provides support for up to 16 analog test points to allow for card monitoring during operation. The following table provides debug module pinout. See card specific documentation for analog test point details.

Table 12: **ADK2 Debug Connector Analog Test Points List**

Pin	Signal Name	Voltage Divider
A29	ADC0_IN0	1
B29	ADC0_IN1	1
A28	ADC0_IN2	1
B28	ADC0_IN3	1
A27	ADC0_IN4	1
B27	ADC0_IN5	1
A26	ADC0_IN6	1
B26	ADC0_IN7	1
A25	ADC1_IN0	1
B25	ADC1_IN1	1

Table 12: **ADK2 Debug Connector Analog Test Points List** *(cont'd)*

Pin	Signal Name	Voltage Divider
A20	ADC1_IN2	1
B20	ADC1_IN3	2
B9	ADC1_IN4	2
A9	ADC1_IN5	2
B1	ADC1_IN6	2
A1	ADC1_IN7	2

GPIO

The debug module supports up to 16 GPIOs. Some of the GPIOs are used for the internal configuration of the debug module. Others are available as reset, control, or general-purpose I/O pins to the card. The following table provides a summary of 16 GPIO signals. The functionality of these signals might differ between cards. See card specific documentation for GPIO details.

Table 13: **Debug Module I/O Expander Control and GPIO list**

I2C MUX	ADK2	Description
MUX_PIO_00	RESERVED	Reserved Must be asserted for proper operation.
MUX_PIO_01	SMARTLYNK_FTDI_JTAG_SEL	0: Selects SmartLynq for AMD device JTAG. 1: Selects FTDI for AMD device JTAG (default).
MUX_PIO_02	IO_EXP_P02_FPGA_SRST	AMD device soft reset. 0: Device in normal operation. 1: Open-drain reset (default).
MUX_PIO_03	IO_EXP_P03_SOC_RST	SoC reset 0: 1: Open-drain reset (default).
MUX_PIO_04	IO_EXP_P04_SUC_RST	SuC reset 0: 1: Open-drain reset (default).
MUX_PIO_05	IO_EXP_P05_DUT_PG_B	Card power cord Input from the card. Asserted when the card is power good.
MUX_PIO_06	USBA_SEL	Reserved
MUX_PIO_07	R_DB_SUC_JTAG_TDI	Reserved
MUX_PIO_10	SUC_UART_EN_B	SuC UART enable 0: SuC UART enabled (default). 1: SuC UART disabled.

Table 13: **Debug Module I/O Expander Control and GPIO list** *(cont'd)*

I2C MUX	ADK2	Description
MUX_PIO_11	FPGA_UART_EN_B	AMD device UART enable 0: AMD device UART enabled (default). 1: AMD device UART disabled.
MUX_PIO_12	SOC_UART_EN_B	SoC UART enable 0: SoC UART enabled (default). 1: SoC UART disabled.
MUX_PIO_13	IO_EXP_P13	GPIO
MUX_PIO_14	IO_EXP_P14	GPIO
MUX_PIO_15	IO_EXP_P15	GPIO
MUX_PIO_16	IO_EXP_P16	0: Mask debug module presence. 1: Allows debug module presence to be advertised card.
MUX_PIO_17	IO_EXP_P17	Reserved

Chapter 6

Environmental

Operating and Storage Temperature Conditions

Table 14: **Operating and Storage Temperatures and Humidity Conditions**

Specification	Condition
Operating temperature	0°C to 55°C
Storage temperature	–40°C to 75°C
Operating humidity, non-condensing	8% to 90%, and a dew point of –12°C
Operating temperature gradient	15°C/hour
Storage humidity, non-condensing	5% to 95%

Regulatory and Compliance Information

Manufacturer Declaration European Community

Regulatory Compliance Markings

When required, these products are provided with the following Product Certification Markings:

- UL Listed Accessories Mark for the USA and Canada
- CE mark

- UKCA mark

Manufacturer Declaration

Xilinx declares that the equipment described in this document is in conformance with the requirements of the European Council Directives listed below:

- RoHS 3 Directive 2011/65/EU, 2015/863
- Reach Regulation 1907/2006
- POP Regulation 2019/1021

This product complies with Directive 2002/95/EC on the restriction of hazardous substances (RoHS) in electrical and electronic equipment.

These products follow the provisions of the European Directive 2014/53/EU.

Dette produkt er i overensstemmelse med det europæiske direktiv 2014/53/EU.

Dit product is in navolging van de bepalingen van Europees Directief 2014/53/EU.

Tämä tuote noudattaa EU-direktiivin 2014/53/EU määräyksiä.

Ce produit est conforme aux exigences de la Directive Européenne 2014/53/EU.

Dieses Produkt entspricht den Bestimmungen der Europäischen Richtlinie 2014/53/EU.

Þessi vara stenst reglugerð Evrópska Efnahags Bandalagsins númer 2014/53/EU.

Questo prodotto è conforme alla Direttiva Europea 2014/53/EU.

Dette produktet er i henhold til bestemmelsene i det europeiske direktivet 2014/53/EU.

Este produto cumpre com as normas da Diretiva Européia 2014/53/EU.

Este producto cumple con las normas del Directivo Europeo 2014/53/EU.

Denna produkt har tillverkats i enlighet med EG-direktiv 2014/53/EU.

This declaration is based upon compliance of the Class A products listed above to the following standards:

EN 55032 (CISPR 32 Class A) RF Emissions Control

EN 55035:2017 (CISPR 35) Electromagnetic compatibility of multimedia equipment – Immunity requirements

EN 62368-1, 2nd Edition, 2014/A11:2017 *Information technology equipment – Safety, Part 1: General Requirements*

CAUTION! *In a domestic environment, Class A products could cause radio interference, in which case the user may be required to take adequate measures.*

ATTENTION! *Dans un environnement domestique, les produits de Classe A peuvent causer des interférences radio, auquel cas l'utilisateur peut être tenu de prendre des mesures adéquates.*

VORSICHT! *In einer häuslichen Umgebung können Produkte der Klasse A Funkstörungen verursachen. In diesem Fall muss der Benutzer möglicherweise geeignete Maßnahmen ergreifen.*

Responsible Party

Xilinx, Inc.
2100 Logic Drive, San Jose, CA 95124
United States of America
Phone: (408) 559-7778

Appendix A

Additional Resources and Legal Notices

Finding Additional Documentation

Documentation Portal

The AMD Adaptive Computing Documentation Portal is an online tool that provides robust search and navigation for documentation using your web browser. To access the Documentation Portal, go to https://docs.xilinx.com.

Documentation Navigator

Documentation Navigator (DocNav) is an installed tool that provides access to AMD Adaptive Computing documents, videos, and support resources, which you can filter and search to find information. To open DocNav:

- From the AMD Vivado™ IDE, select **Help → Documentation and Tutorials**.
- On Windows, click the **Start** button and select **Xilinx Design Tools → DocNav**.
- At the Linux command prompt, enter `docnav`.

***Note*:** For more information on DocNav, refer to the *Documentation Navigator User Guide* (UG968).

Design Hubs

AMD Design Hubs provide links to documentation organized by design tasks and other topics, which you can use to learn key concepts and address frequently asked questions. To access the Design Hubs:

- In DocNav, click the **Design Hubs View** tab.
- Go to the Design Hubs web page.

Support Resources

For support resources such as Answers, Documentation, Downloads, and Forums, see Support.

References

These documents provide supplemental material useful with this guide:

1. Alveo Debug Kit - Master Answer Record
2. https://www.segger.com/products/debug-probes/j-link/
3. https://www.nxp.com/design/microcontrollers-developer-resources/lpc-link2:OM13054
4. https://www.ti.com/tool/MSP-FET
5. https://www.totalphase.com/products/aardvark-i2cspi/
6. https://www.totalphase.com/products/beagle-i2cspi/
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8. AMD SmartLynq Data Cable
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Revision History

The following table shows the revision history for this document.

Section	Revision Summary
09/29/2023 Version 1.3	
Initial public release.	N/A
01/27/2023 Version 1.2	
Supported Cards	Minor grammar edit.
08/01/2022 Version 1.1	
Supported Cards	Added reference.
05/26/2022 Version 1.0	
AMD Confidential Draft. Approved for external release under NDA only.	N/A

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