

ML62Q1300 Group

16-bit micro controller

GENERAL DESCRIPTION

ML62Q1300 Group is a high performance CMOS 16-bit microcontroller equipped with an 16-bit CPU nX-U16/100 and integrated with program memory(Flash memory), data memory(RAM), data Flash and rich peripheral functions such as the multiplier/divider, CRC operator, DMA controller, clock generator, timer, UART, synchronous serial port, I²C bus interface unit, buzzer, Voltage Level Supervisor(VLS), successive approximation type A/D converter, D/A converter, analog comparator, safety function and etc.

The CPU nX-U16/100 is capable of efficient instruction execution in 1-instruction 1-clock mode by pipeline architecture parallel processing.

The built-in on-chip debug function enables debugging and programming the software. Also, ISP(In-System Programming) function supports the Flash programming in production line.

The ML62Q1300 Group has five packages (16pin - 32pin) and five kinds of memory sizes(16Kbyte - 64Kbyte).

Table 1 ML62Q1300 Group Product List

Program memory	Data memory (RAM)	Data Flash	16pin SSOP16 WQFN16	20pin TSSOP20	24pin WQFN24	32pin TQFP32 WQFN32
64Kbyte	4Kbyte	2Kbyte	—	—	ML62Q1347	ML62Q1367
48Kbyte			—	—	ML62Q1346	ML62Q1366
32Kbyte			—	—	ML62Q1345	ML62Q1365
32Kbyte	2Kbyte		ML62Q1325	ML62Q1335	—	—
24Kbyte			ML62Q1324	ML62Q1334	—	—
16Kbyte			ML62Q1323	ML62Q1333	—	—

FEATURES

- CPU
 - 16-bit RISC CPU (CPU name: nX-U16/100)
 - Instruction system: 16-bit length instruction
 - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
 - On-chip debug function built-in (supported by LAPIS on-chip debug emulator EASE1000)
 - ISP (In-System Programming) function built-in
 - Minimum instruction execution time
30.5 μs (at 32.768 KHz system clock)
62.5ns/41.6ns (at 16 MHz/24MHz system clock)
- Coprocessor for multiplication and division
 - Multiplication: 16bit × 16bit (operation time 4 cycles)
 - Division: 32bit / 16bit (operation time 8 cycles)
 - Division: 32bit / 32bit (operation time 16 cycles)
 - Multiply-accumulate (non-saturating): 16bit × 16bit + 32bit (operation time 4 cycles)
 - Multiply-accumulate (saturating): 16bit × 16bit + 32bit (operation time 4 cycles)

- Operating voltage and temperature
 - Operating voltage: $V_{DD} = 1.6$ to 5.5 V (Need 1.8 V or higher at the power on)
 - Operating temperature: -40 to $+105$ °C
- Internal memory
 - Program Flash memory area
 - Rewrite count: 100 cycles
 - Rewrite unit: 32bit(4byte)
 - Erase unit: 16Kbyte/1Kbyte
 - Erase/Rewrite temperature: 0°C to $+40^{\circ}\text{C}$
 - Data Flash memory area
 - Rewrite count 10,000 cycles
 - Rewrite unit: 8bit(1byte)
 - Erase unit: 2Kbyte/128byte
 - Erase/Rewrite temperature: -40°C to $+85^{\circ}\text{C}$
 - Back Ground Operation(CPU can work while erasing and rewriting)
 - Data RAM area
 - Rewrite unit: 8bit/16bit(1byte/2byte)
 - Parity check function (Parity error reset or interrupt is generatable)
- Clock
 - Low-speed clock
 - Internal low-speed RC oscillation: Approx.32.768 KHz
 - High-speed clock
 - PLL oscillation: 24MHz/16MHz is selectable by code option
 - WDT(Watch Dog Timer) clock
 - Internal low-speed RC oscillation: Approx. 1kHz
 - The WDT independent clock or the divided clock of internal low-speed clock is selectable by the code option.
- Reset
 - RESET_N pin reset
 - Reset by power-on detection
 - Reset by the 2nd watchdog timer (WDT) overflow
 - Reset by WDT counter clear during the clear invalid period
 - Reset by RAM parity error
 - Reset by unused ROM access
 - Reset by voltage level detection (VLS)
 - The software reset by BRK instruction (reset CPU only)
 - Reset to the peripheral circuits by Block Reset Control Registers (BRECON 0 to 3)

- Power management
 - HALT mode: CPU stops executing instruction, clock oscillations and peripheral circuits remain previous states
 - HALT-H mode: CPU stops executing instruction, high-speed clock oscillation stops and peripheral circuits working with low-speed clock remain previous states
 - STOP mode: CPU stops executing instruction, both high-speed oscillation and low-speed oscillation stop.
 - STOP-D mode: CPU stops executing instruction, both high-speed oscillation and low-speed oscillation stop. The internal regulator's output voltage (V_{DDL}) goes down to reduce the current consumption.
 - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, 1/8, 1/16 or 1/32 of the oscillation clock)
 - Block Control Function: Powers down the circuits of unused function blocks (reset the block or stop supplying the clock)
- Interrupt controller
 - Non-maskable interrupt source: 1 (Internal sources: WDT)
 - Maskable interrupt sources: max.24
 - Four step interrupt levels
 - External interrupt ports : max 8
- Watchdog timer(WDT)
 - Operation clock: 1kHz WDT independent clock or 32.768kHz RC oscillation clock, selectable by code option
 - Overflow period: 8 types selectable (7.8ms, 15.6ms, 31.3ms, 62.5ms, 125ms, 500ms, 2000ms and 8000ms @32.768kHz)
 - WDT counter clear enable period : 50%, 75% or 100% of overflow period
 When 100% of overflow period is selected,
 The first overflow generates an interrupt, and the second overflow generates a reset.
 When 50% or 70% of overflow period is selected,
 The first overflow generates a reset.
 Clearing the WDT counter out of the enable period generates the WDT invalid clear reset.
 - WDT operation : Enable or disable is selectable by code option
 - Readable WDT counter (WDT counter monitor function)
- DMA(Direct Memory Access) controller
 - Channel : 2ch
 - Transfer unit: 8bit/16bit
 - Max. transfer count: 1024 time
 - Transfer type: 2 cycle transfer
 - Transfer mode: Single transfer mode
 Fixed address, address increments and address decrements
 - Transfer target: SFR/RAM $\leftrightarrow$ SFR/RAM (Transfer from/to Flash is not supported)
 - Transfer request: Serial unit interrupt, A/D interrupt and 16bit timer interrupt, Functional timer interrupt, External interrupt.
- Time base counter
 - Divide the Low-speed clock(LSCLK) and generate 32.768kHz-1Hz internal pulse signals
 - Periodical interrupt $\times$ 3 selectable from 8 frequencies (128Hz, 64Hz, 32Hz, 16Hz, 8Hz, 4Hz, 2Hz and 1Hz)
 - The time base clock output (1Hz or 2Hz) from general purpose ports (TBCOUT1).
- Functional timer(FTM)
 - Channel: 4ch
 - Timer one shot mode and repeat mode, Capture mode, PWM mode1 and PWM mode 2(complementary output)
 - Same start/stop is available with different channels
 (This function is not available with 16bit General Timer)
 - Event trigger (external interrupts, analog comparator interrupts, 16bit general timer interrupts and Functional timer interrupts)
 - Delay counter (for generating dead time)
 - Available to specify division ratio of counter clock channel by channel

- 16bit General timers
 - Channel: 6ch
 - 8 bits timer mode and 16-bit timer mode (1ch 16-bit timer is configurable as 2ch 8-bit timer)
 - Same start/stop is available with different channels
(This function is not available with Functional Timer)
 - Timer output (toggled by overflow)
 - Available to specify division ratio of counter clock channel by channel
- Serial communication unit
 - Channel: Max. 2ch
 - Synchronous Serial Port or UART is selectable in each channel

< Synchronous Serial Port >

 - Master/slave selectable
 - LSB first/MSB first selectable
 - 8-bit length/16-bit length selectable

< UART >

 - Full-duplex communication x 1ch(One Full-duplexUART is configurable as two half-duplex UARTs)
 - 5-8 bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
 - Positive logic/negative logic selectable
 - LSB first/MSB first selectable
 - Internal baud rate generator (~ 2Mbps)
- I²C bus interface unit (Master/Slave)
 - Channel: 1ch
 - Master or Slave mode is selectable

< Master function >

 - Standard mode (100 kbit/s), fast mode (400 kbit/s) and 1Mbps mode(1Mbit/s)
 - Handshake (Clock synchronization)
 - 7bit address format (10bit address format is supported)

< Slave function >

 - Standard mode (100 kbit/s), fast mode (400 kbit/s) and 1Mbps mode(1Mbit/s)
 - Handshake (Clock synchronization)
 - 7bit address format
- I²C bus interface (Master only)
 - Channel: 1ch
 - Standard mode (100 kbit/s), fast mode (400 kbit/s) and 1Mbps mode(1Mbit/s)
 - Handshake (Clock synchronization)
 - 7bit address format (10bit address format is supported)
- General-purpose ports (GPIO)
 - I/O port: Max. 28 (Including one pin for on-chip debug and pins for other shared functions)
 - External interrupt function × 8
 - LED driver port : Max. 27
 - Carrier frequency output function (used for IR communication)
- Successive approximation type A/D converter
 - Channel: Max.8ch
 - Resolution: 10bit
 - Conversion time: Selectable 2.25μs (min) /channel (When the conversion clock is 8MHz)
 - Reference voltages are selectable
(V_{DD} pin input voltage / Internal reference voltage(Approx. 1.55V) / External reference voltage (V_{REF} pin)
 - Scan function (repeat conversion)
 - One result register for each channel
 - Interrupt by threshold of conversion result

- Temperature sensor for low-speed RC oscillation adjustment
- Voltage level supervisor (VLS)
 - Accuracy: $\pm 4^{\circ}\text{C}$
 - Threshold voltage: 12 values selectable (1.85V ~ 4.00V)
 - Voltage level detection reset (VLS reset)
 - Voltage level detection interrupt (VLS0 interrupt)
- Analog comparator
 - Channel: 1ch
 - Interrupts allow edge selection and sampling selection
 - An external or an internal reference voltage is selectable
- D/A converter
 - Channel: Max 1ch
 - Resolution: 8bit
 - Output impedance: 6k ohm(Typ.)
 - R-2R ladder method
- Buzzer
 - 4 buzzer mode (Repeat sound, Single sound, Intermittent sound 1 and Intermittent sound 2)
 - 8 frequencies (4.096kHz to 293Hz)
 - 15 step duty (1/16 to 15/16)
 - Selectable the logic of buzzer output pin (Positive or Negative logic)
- CRC(Cyclic Redundancy Check) operation function
 - Generation equation: $X^{16}+X^{12}+X^5+1$
 - LSB first or MSB first is selectable
 - Automatic CRC mode: Automatic CRC calculation with data of program memory in HALT mode
- Safety Function
 - RAM/SFR guard
 - Automatic CRC calculation with data of program memory
 - RAM parity error detection
 - ROM unused area access reset
 - Clock mutual check
 - WDT counter check
 - Successive approximation type A/D converter test
 - UART test
 - Synchronous serial test
 - I²C test
 - GPIO test

- Shipping package (TBD.)
 - 16-pin plastic SSOP
ML62Q1323/1324/1325 - xxxMB (Blank part: ML62Q1323/1324/1325-NNNMB)
 - 16-pin plastic WQFN
ML62Q1323/1324/1325 - xxxGD (Blank part: ML62Q1323/1324/1325-NNNGD)
 - 20-pin plastic TSSOP
ML62Q1333/1334/1335 - xxxTD
(Blank part: ML62Q1333/1334/1335-NNNTD)
 - 24-pin plastic WQFN
ML62Q1345/1346/1347 - xxxGD
(Blank part: ML62Q1345/1346/1347-NNNGD)
 - 32-pin plastic TQFP
ML62Q1365/1366/1367 - xxxTB
(Blank part: ML62Q1365/1366/1367-NNNTB)
 - 32-pin plastic WQFN
ML62Q1365/1366/1367 - xxxGD
(Blank part: ML62Q1365/1366/1367-NNNGD)

xxx: ROM code number

ML62Q1300 Group how to read the part number

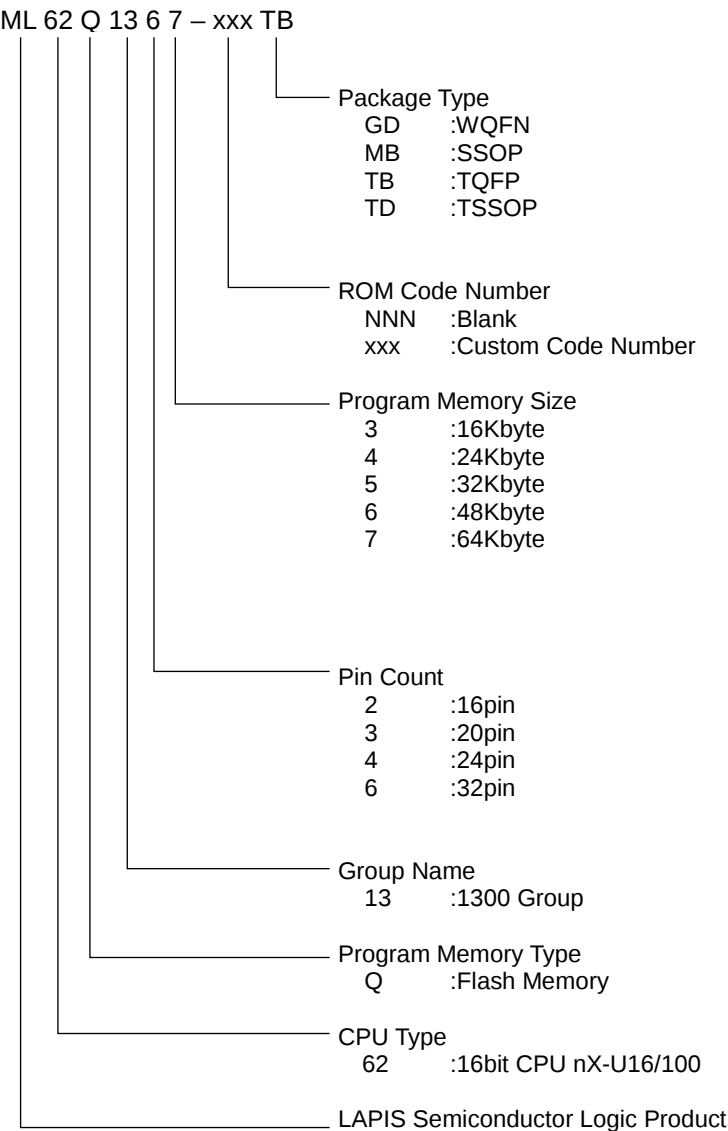


Figure 1 ML62Q1300 Group Part Number

ML62Q1300 Group Main Function List

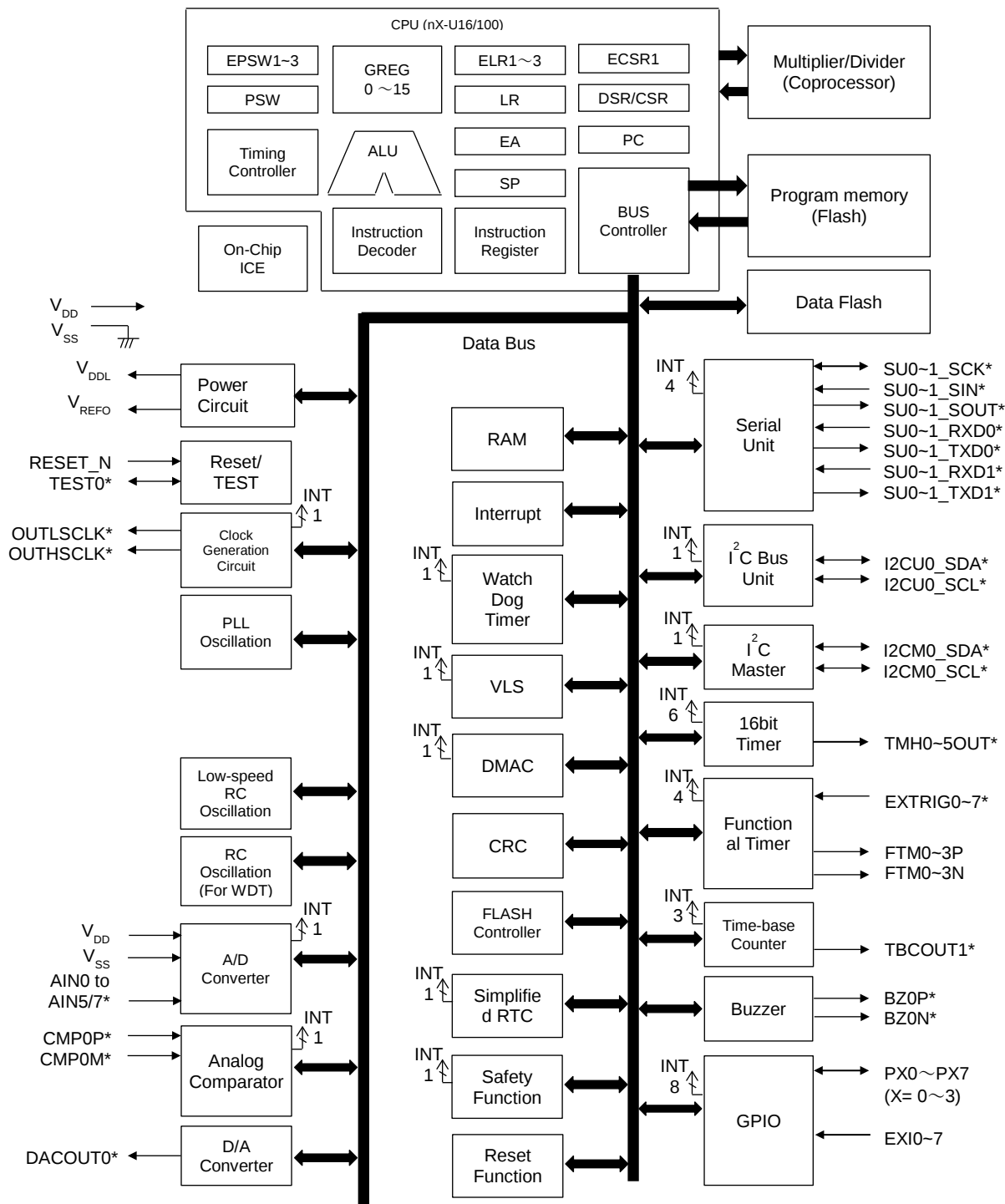
Table 2 ML62Q1300 Group Main Function List

Table 2 ML62Q1366 Group Main Function List																	
Part number	Pin				Interrupt	Timer		Serial		Analog							
	Total pin-counts	Power pin counts	Reset Input pin	I/O port	LED drive port	Internal interrupt [source]	External interrupt [port]	Functional Timer [channel]	16bit General I Timer [channel] * ¹	Simplified RTC [channel]	Full-duplex UART or Synchronous serial [channel] * ²	I ² C bus unit (Master/Slave) [channel]	I ² C bus interface (Master only) [channel]	10bit Successive type A/D converter [channel]	Analog comparator [channel]	Analog comparator [input pin]	8bit D/A converter [channel]
ML62Q1323	16	3	1	12	11	22	8	4	4	0	2	1	1	6	1	2	0
ML62Q1324																	
ML62Q1325																	
ML62Q1333	20			16	15	24			6								
ML62Q1334																	
ML62Q1335																	
ML62Q1345	24			20	19	27											
ML62Q1346																	
ML62Q1347																	
ML62Q1365	32			28													
ML62Q1366																	
ML62Q1367																	

*¹ : One 16bit timer is configurable as two 8bit timers

*² : Full-duplex UART and Synchronous Serial Port can not be used simultaneously in the same channel.
One Full-duplexUART is configurable as two half-duplex UARTs.

BLOCK DIAGRAM



* : indicates the shared function of general ports.

Figure 2 ML62Q1300 Group Block Diagram

PIN CONFIGURATION

Pin Layout of ML62Q1323/1324/1325 16pin SSOP Package

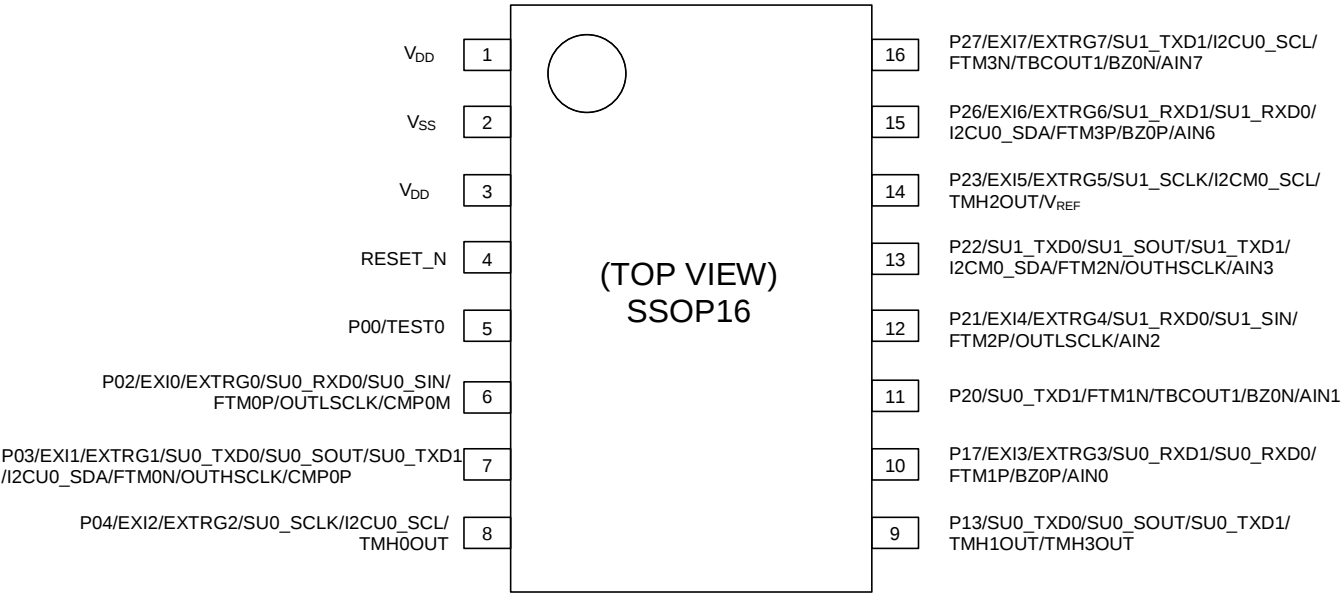


Figure 3 Pin Layout of 16pin SSOP Package

Pin Layout of ML62Q1323/1324/1325 16pin WQFN Package

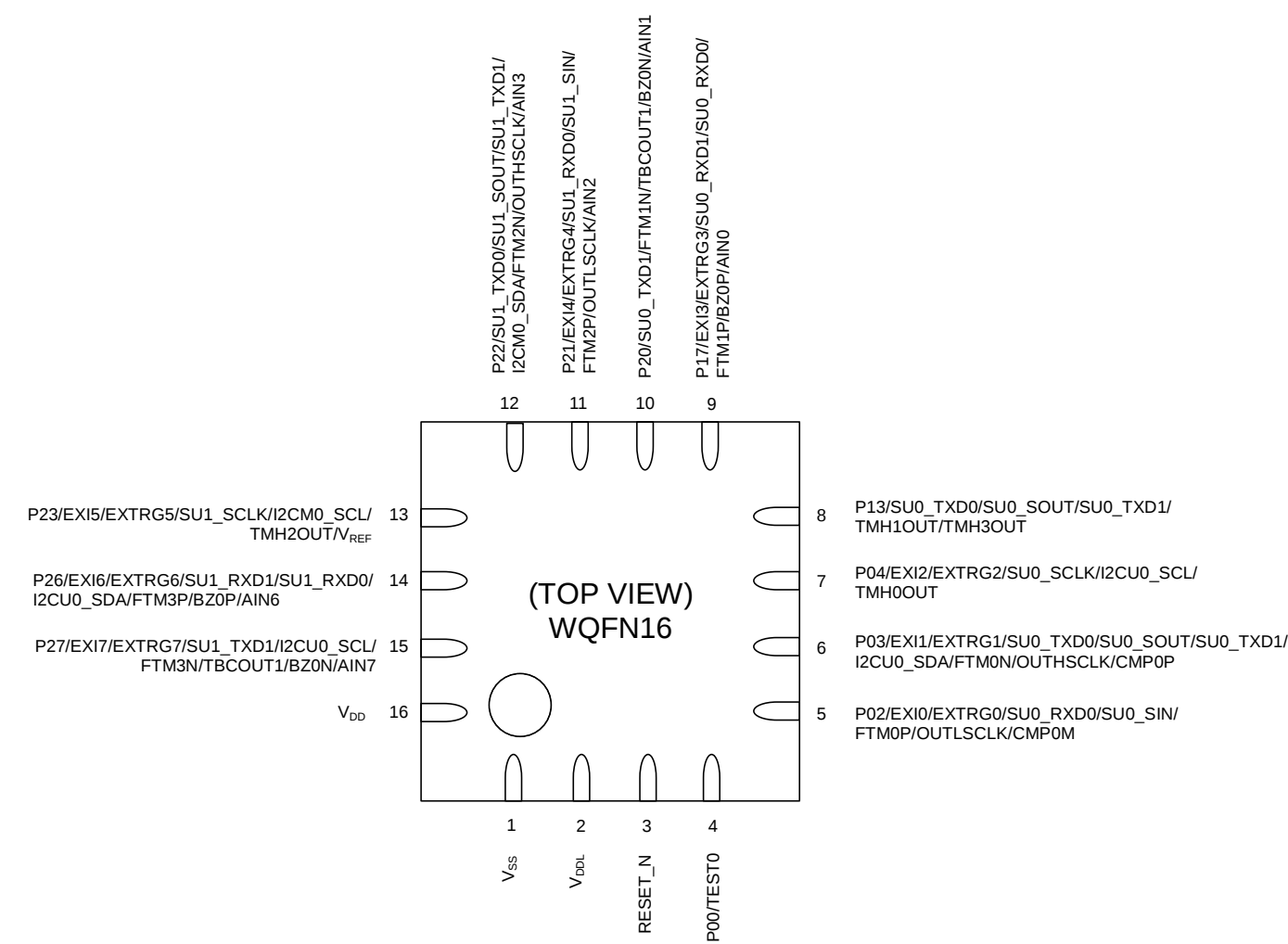


Figure 4 Pin Layout of 16pin WQFN Package

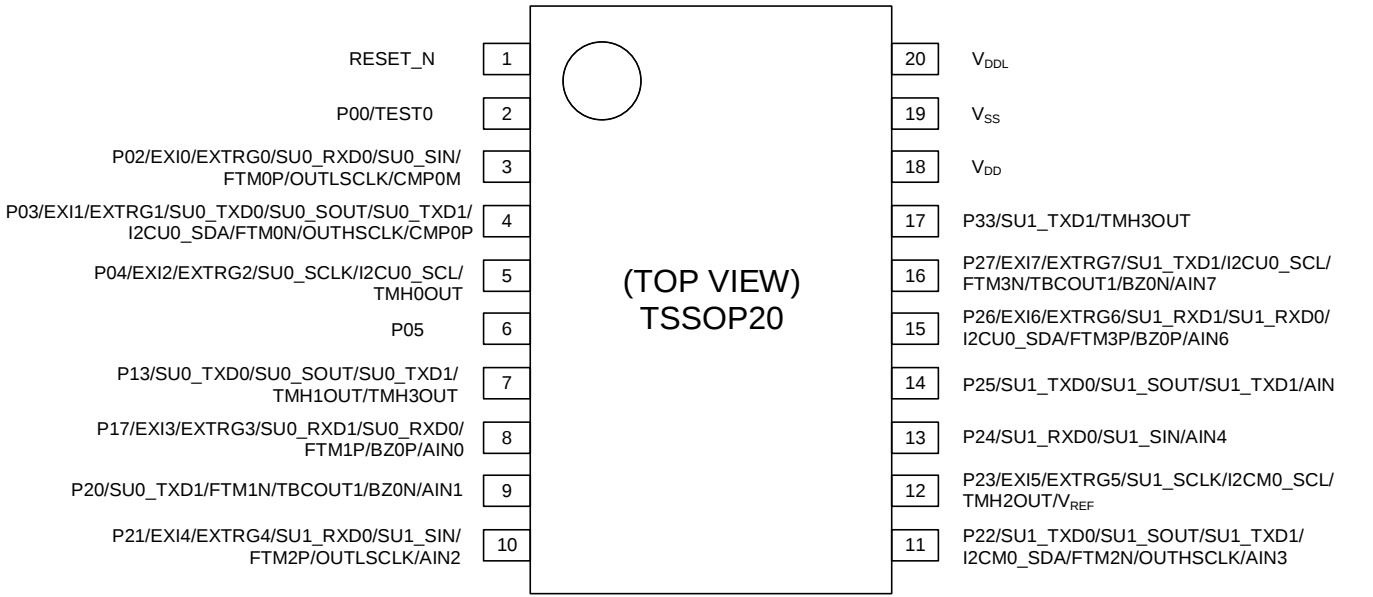


Figure 5 Pin Layout of 20pin TSSOP Package

Pin Layout of ML62Q1345/1346/1347 24pin WQFN Package

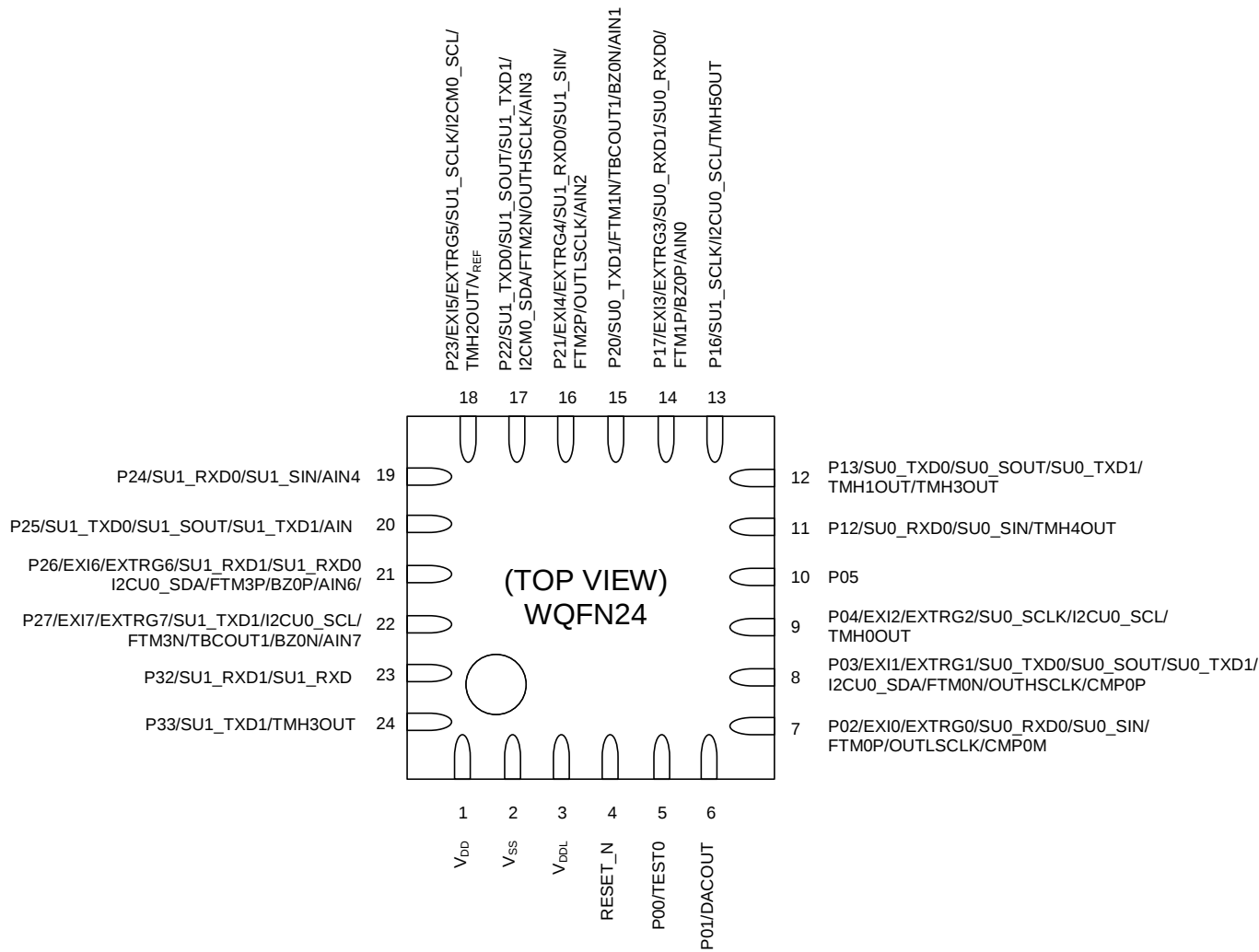


Figure 6 Pin Layout of 24pin WQFN Package

Pin Layout of ML62Q1365/1366/1367 32pin TQFP Package

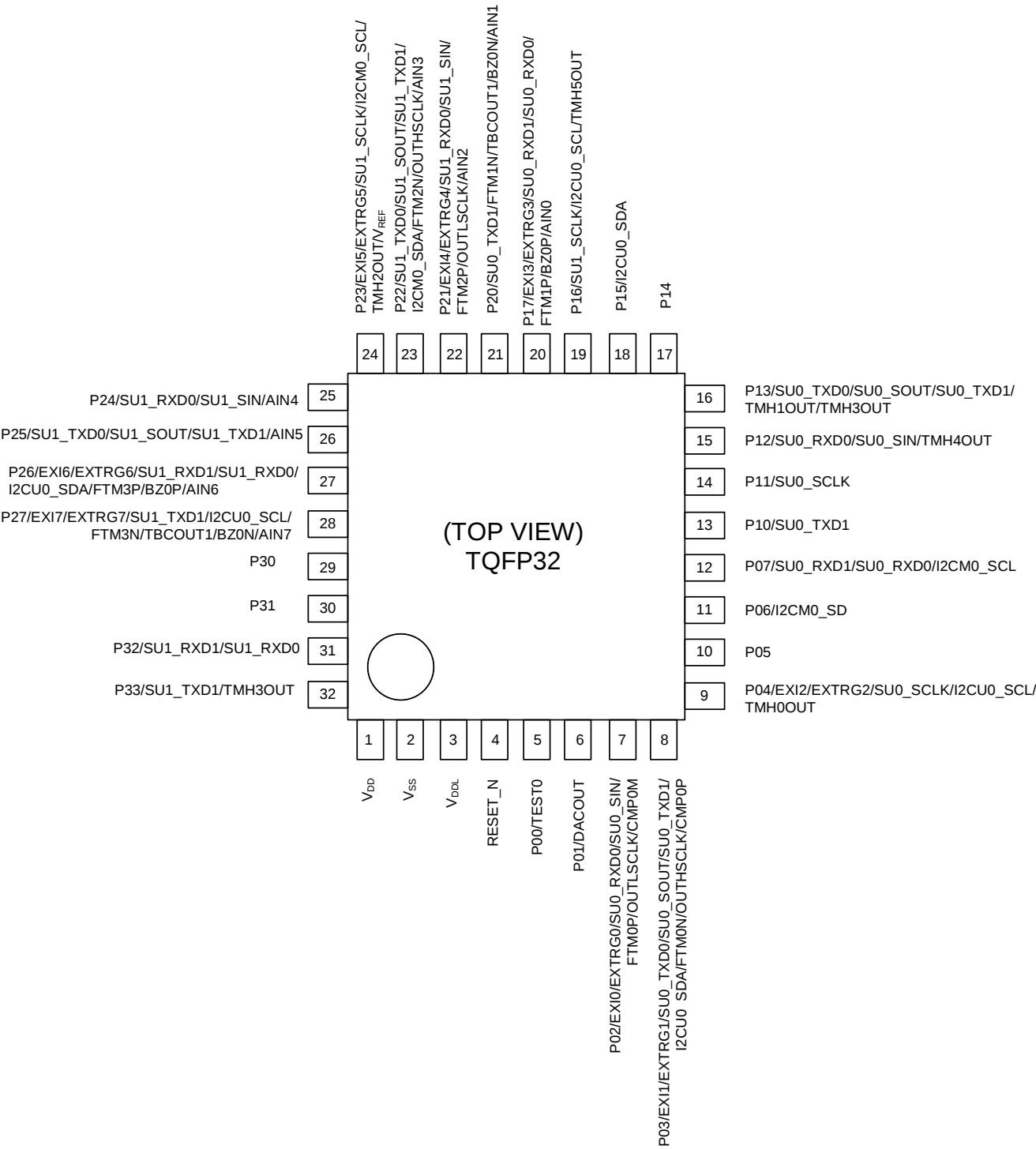


Figure 7 Pin Layout of 32pin TQFP Package

Pin Layout of ML62Q1365/1366/1367 32pin WQFN Package

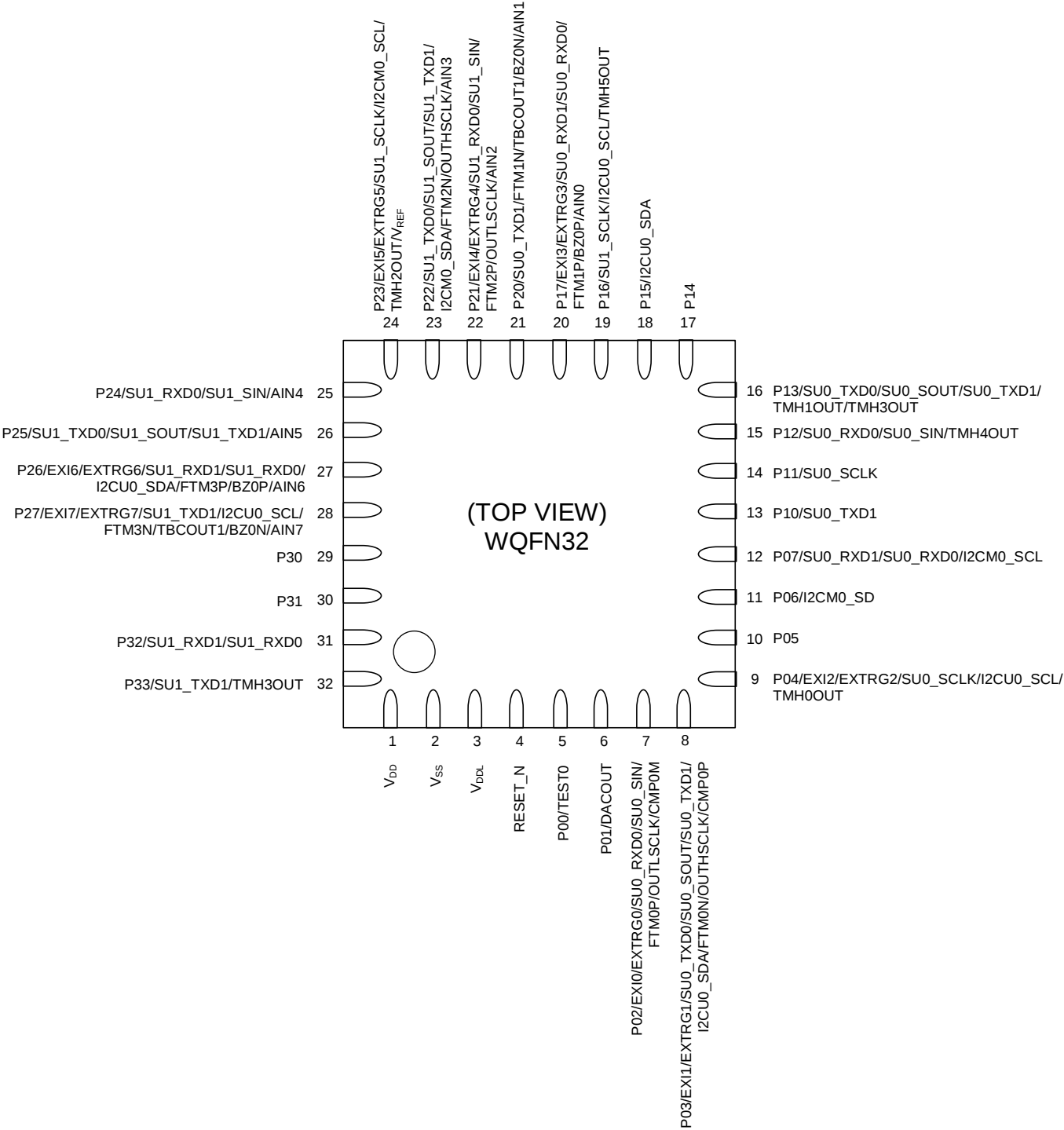


Figure 8 Pin Layout of 32pin WQFN Package

PIN LIST

Table 3 Pin List (1/7)

16Pin No.(SSOP)	16Pin No.(MQFN)	20Pin No.(TSSOP)	24Pin No.(MQFN24)	32Pin No.(TQFP) (MQFN)	Pin name	Primary function	Shared function	
1	16	18	1	1	V _{DD}	Positive power pin	—	
2	1	19	2	2	V _{SS}	Negative power pin	—	
3	2	20	3	3	V _{DDL}	Internal regulator output	—	
4	3	1	4	4	RESET_N(I)	Reset input Used for on-chip debug interface	—	
5	4	2	5	5	P00 / TEST0 (I/O)	General I/O pin Used for on-chip debug interface (Not available to use as I/O pin when connecting to the on-chip emulator)	—	
-	-	-	6	6	P01 / DACOUT0 (I/O)	General I/O pin D/A converter0 output pin	2 nd function	—
							3 rd function	—
							4 nd function	—
							5 nd function	—
							6 nd function	—
							7 nd function	—
							8 nd function	—
6	5	3	7	7	P02 / EXI0 / EXTRG0 (I/O)	General I/O pin D/A converter output pin	2 nd function	SU0_RXD0/SU0_SIN
							3 rd function	—
							4 nd function	—
							5 nd function	FTM0P
							6 nd function	OUTLSCLK
							7 nd function	CMP0M
							8 nd function	—
7	6	4	8	8	P03 / EXI1 / EXTRG1 (I/O)	General I/O pin External interrupt Functional timer external trigger	2 nd function	SU0_TXD0/SU0_SOUT
							3 rd function	SU0_TXD1
							4 nd function	I2CU0_SDA
							5 nd function	FTM0N
							6 nd function	OUTHCLK
							7 nd function	CMP0P
							8 nd function	—

Table 3 Pin List (2/7)

					Pin name	Primary function	Shared function	
16Pin No.(SSOP)	16Pin No.(WQFN)	20Pin No.(TSSOP)	24Pin No.(WQFN24)	32Pin No.(TQFP) (WQFN)				
8	7	5	9	9	P04 / EXI2 / EXTRG2 (I/O)	General I/O pin External interrupt Functional timer external trigger	2 nd function	SU0_SCLK
							3 rd function	—
							4 nd function	I2CU0_SCL
							5 nd function	TMH0OUT
							6 nd function	—
							7 nd function	—
							8 nd function	—
							8 nd function	—
-	-	6	10	10	P05 (I/O)	General I/O pin	2 nd function	—
							3 rd function	—
							4 nd function	—
							5 nd function	—
							6 nd function	—
							7 nd function	—
							8 nd function	—
							8 nd function	—
-	-	-	-	11	P06 (I/O)	General I/O pin	2 nd function	—
							3 rd function	—
							4 nd function	I2CM0_SDA
							5 nd function	—
							6 nd function	—
							7 nd function	—
							8 nd function	—
							8 nd function	—
-	-	-	-	12	P07 (I/O)	General I/O pin	2 nd function	SU0_RXD1
							3 rd function	SU0_RXD0
							4 nd function	I2CM0_SCL
							5 nd function	—
							6 nd function	—
							7 nd function	—
							8 nd function	—
							8 nd function	—

Table 3 Pin List (3/7)

16Pin No.(SSOP)	16Pin No.(WQFN)	20Pin No.(TSSOP)	24Pin No.(WQFN24)	32Pin No.(TQFP) (WQFN)	Pin name	Primary function	Shared function	
							2 nd function	
-	-	-	-	13	P10 (I/O)	General I/O pin	SU0_TXD1	
							3 rd function	—
							4 nd function	—
							5 nd function	—
							6 nd function	—
							7 nd function	—
							8 nd function	—
-	-	-	-	14	P11 (I/O)	General I/O pin	SU0_SCLK	
							3 rd function	—
							4 nd function	—
							5 nd function	—
							6 nd function	—
							7 nd function	—
							8 nd function	—
-	-	-	11	15	P12 (I/O)	General I/O pin	SU0_RXD0/SU0_SIN	
							3 rd function	—
							4 nd function	—
							5 nd function	TMH4OUT
							6 nd function	—
							7 nd function	—
							8 nd function	—
9	8	7	12	16	P13 (I/O)	General I/O pin	SU0_TXD0/SU0_SOUT	
							SU0_TXD1	
							4 nd function	—
							5 nd function	TMH1OUT
							6 nd function	—
							7 nd function	TMH3OUT
							8 nd function	—

Table 3 Pin List (4/7)

16Pin No.(SSOP)	16Pin No.(WQFN)	20Pin No.(TSSOP)	24Pin No.(WQFN24)	32Pin No.(TQFP) (WQFN)	Pin name	Primary function	Shared function	
							2 nd function	—
-	-	-	-	17	P14 (I/O)	General I/O pin	3 rd function	—
							4 nd function	—
							5 nd function	—
							6 nd function	—
							7 nd function	—
							8 nd function	—
							2 nd function	—
-	-	-	-	18	P15 (I/O)	General I/O pin	3 rd function	—
							4 nd function	I2CU0_SDA
							5 nd function	—
							6 nd function	—
							7 nd function	—
							8 nd function	—
-	-	-	13	19	P16 (I/O)	General I/O pin	2 nd function	SU1_SCLK
							3 rd function	—
							4 nd function	I2CU0_SCL
							5 nd function	TMH5OUT
							6 nd function	—
							7 nd function	—
							8 nd function	—
10	9	8	14	20	P17 / EXI3/ EXTRG3 (I/O)	General I/O pin External interrupt Functional timer external trigger	2 nd function	SU0_RXD1
							3 rd function	SU0_RXD0
							4 nd function	—
							5 nd function	FTM1P
							6 nd function	TBCOUT0
							7 nd function	BZ0P
							8 nd function	AIN0

Table 3 Pin List (5/7)

16Pin No.(SSOP)	16Pin No.(WQFN)	20Pin No.(TSSOP)	24Pin No.(WQFN24)	32Pin No.(TQFP) (WQFN)	Pin name	Primary function	Shared function	
11	10	9	15	21	P20 (I/O)	General I/O pin	2 nd function	SU0_TXD1
							3 rd function	—
							4 nd function	—
							5 nd function	FTM1N
							6 nd function	TBCOUT1
							7 nd function	BZ0N
							8 nd function	AIN1
12	11	10	16	22	P21 / EXI4 / EXTRG4 (I/O)	General I/O pin External interrupt Functional timer external trigger	2 nd function	SU1_RXD0/SU1_SIN
							3 rd function	—
							4 nd function	—
							5 nd function	FTM2P
							6 nd function	OUTLSCLK
							7 nd function	—
13	12	11	17	23	P22 (I/O)	General I/O pin	2 nd function	SU1_TXD0/SU1_SOUT
							3 rd function	SU1_TXD1
							4 nd function	I2CM0_SDA
							5 nd function	FTM2N
							6 nd function	OUTHCLK
							7 nd function	—
14	13	12	18	24	P23 / EXI5 / EXTRG5 V _{REF} (I/O)	General I/O pin External interrupt Functional timer external trigger. SA type A/D converter external reference voltage input.	2 nd function	SU1_SCLK
							3 rd function	—
							4 nd function	I2CM0_SCL
							5 nd function	TMH2OUT
							6 nd function	—
							7 nd function	—
							8 nd function	V _{REF0}

Table 3 Pin List (6/7)

16Pin No.(SSOP)	16Pin No.(WQFN)	20Pin No.(TSSOP)	24Pin No.(WQFN24)	32Pin No.(TQFP) (WQFN)	Pin name	Primary function	Shared function	
							2 nd function	3 rd function
-	-	13	19	25	P24 (I/O)	General I/O pin	SU1_RXD0/SU1_SIN	—
							4 nd function	—
							5 nd function	—
							6 nd function	—
							7 nd function	—
							8 nd function	AIN4
-	-	14	20	26	P25 (I/O)	General I/O pin	2 nd function	SU1_TXD0/SU1_SOUT
							3 rd function	SU1_TXD1
							4 nd function	—
							5 nd function	—
							6 nd function	—
							7 nd function	—
							8 nd function	AIN5
15	14	15	21	27	P26 / EXI6 / EXTRG6 (I/O)	General I/O pin External interrupt Functional timer external trigger	2 nd function	SU1_RXD1
							3 nd function	SU1_RXD0
							4 nd function	I2CU0_SDA
							5 nd function	FTM3P
							6 nd function	—
							7 nd function	BZ0P
							8 nd function	AIN6
16	15	16	22	28	P27 / EXI7 / EXTRG7 (I/O)	General I/O pin External interrupt Functional timer external trigger	2 nd function	SU1_TXD1
							3 rd function	—
							4 nd function	I2CU0_SCL
							5 nd function	FTM3N
							6 nd function	TBCOUT1
							7 nd function	BZ0N
							8 nd function	AIN7

Table 3 Pin List (7/7)

16Pin No.(SSOP)	16Pin No.(WQFN)	20Pin No.(TSSOP)	24Pin No.(WQFN24)	32Pin No.(TQFP) (WQFN)	Pin name	Primary function	Shared function	
							2 nd function	—
-	-	-	-	29	P30 (I/O)	General I/O pin	3 rd function	—
							4 nd function	—
							5 nd function	—
							6 nd function	—
							7 nd function	—
							8 nd function	—
							2 nd function	—
-	-	-	-	30	P31 (I/O)	General I/O pin	3 rd function	—
							4 nd function	—
							5 nd function	—
							6 nd function	—
							7 nd function	—
							8 nd function	—
-	-	-	23	31	P32 (I/O)	General I/O pin	2 nd function	SU1_RXD1
							3 rd function	SU1_RXD0
							4 nd function	—
							5 nd function	—
							6 nd function	—
							7 nd function	—
							8 nd function	—
-	-	17	24	32	P33 (I/O)	General I/O pin	2 nd function	SU1_TXD1
							3 rd function	—
							4 nd function	—
							5 nd function	TMH3OUT
							6 nd function	—
							7 nd function	—
							8 nd function	—

PIN DESCRIPTION

Table 4 Pin Description (1/4)

Function	Signal name	Pin name	I/O	Description	Logic
Power	—	V _{SS}	—	Negative power supply pin (-)	—
	—	V _{DD}	—	Positive power supply pin (+). Connect a capacitor C _V (1μF) between this pin and V _{SS} .	—
	—	V _{DDL}	—	Power supply pin for internal logic (internal regulator's output). Connect a capacitor C _V (1μF) between this pin and V _{SS} .	—
Test	TEST0	P00	I/O	Input pin for testing. Also, used for on-chip debug interface or ISP function. P00 is initialized as pull-up input mode by the system reset (not high-impedance mode).	Positive
System	V _{REFO}	P23	—	Reference voltage output. An internal reference voltage in the SA type A/D converter block can be externally used for a reference. The pin is shared with the SA type A/D converter external reference voltage input.	—
	RESET_N	RESET_N	I	Input for reset. Asserting "L" level to this pin enters the MCU into system reset mode and internal circuits are initialized, then releasing it to "H" level make CPU start running the program. Used for on-chip debug interface or ISP function. Internal pull-up resistor is not installed.	Negative
	OUTLSCLK	P02	O	Low-speed clock output.	—
		P21			
	OUTHCLK	P03	O	Low-speed clock output.	—
		P22			
General port (GPIO)	P00	P00	I/O	General I/O port - High-impedance - Input with Pull-UP (initial value) - Input without Pull-UP - CMOS output - N-channel open drain output P00 is only initialized as pulled-up input and other ports are initialized as high-impedance Not available to use as I/O pin when using for on-chip debug interface or ISP function.	Positive
	P01 – P07	P01 – P07	I/O	General I/O port - High-impedance (initial value) - Input with Pull-UP - Input without Pull-UP - CMOS output - N-channel open drain output	Positive
	P10 – P17	P10 – P17			
	P20 – P27	P20 – P27			
	P30 – P33	P30 – P33			

Table 4 Pin Description (2/4)

Function	Signal name	Pin name	I/O	Description	Logic
UART	SU0_TXD0	P03	O	Serial communication unit0/UART0 data output pin.	Positive
		P13			
	SU0_RXD0	P02	I	Serial communication unit0/UART0 data input pin.	Positive
		P07			
		P12			
		P17			
	SU0_TXD1	P03	O	Serial communication unit0/UART1 data output pin.	Positive
		P10			
		P13			
		P20			
	SU0_RXD1	P07	I	Serial communication unit0/UART1 data input pin.	Positive
		P17			
	SU1_TXD0	P22	O	Serial communication unit1/UART0 data output pin.	Positive
		P25			
	SU1_RXD0	P21	I	Serial communication unit1/UART0 data input pin.	Positive
		P24			
		P26			
		P32			
	SU1_TXD1	P22	O	Serial communication unit1/UART1 data output pin.	Positive
		P25			
		P27			
		P33			
	SU1_RXD1	P26	I	Serial communication unit1/UART1 data input pin.	Positive
		P32			
Synchronous Serial Port	SU0_SIN	P02	I	Serial communication unit0/Synchronous serial data input pin.	Positive
		P12			
	SU0_SCK	P04	I/O	Serial communication unit0/Synchronous serial clock I/O pin.	Positive
		P11			
	SU0_SOUT	P03	O	Serial communication unit0/Synchronous serial data output pin.	Positive
		P13			
I ² C Bus	I2CU0_SDA	P03	I/O	I ² C Unit0 (Master and Salve) Data I/O pin / N-ch open drain. Connect a pull-up resistor externally.	Positive
		P15			
		P26			
	I2CU0_SCL	P04	I/O	I ² C Unit0 (Master and Salve) Clock I/O pin / N-ch open drain. Connect a pull-up resistor externally.	Positive
		P16			
		P27			
	I2CM0_SDA	P06	I/O	I ² C Master0 Data I/O pin / N-ch open drain. Connect a pull-up resistor externally.	Positive
		P22			
	I2CM0_SCL	P07	I/O	I ² C Master0 Clock I/O pin / N-ch open drain. Connect a pull-up resistor externally.	Positive
		P23			

Table 4 Pin Description (3/4)

Function	Signal name	Pin name	I/O	Description	Logic
Functional Timer (FTM)	FTM0P	P02	O	Functional Timer0 output.	Positive
	FTM0N	P03	O	Functional Timer0 output.	Negative
	FTM1P	P17	O	Functional Timer1 output.	Positive
	FTM1N	P20	O	Functional Timer1 output.	Negative
	FTM2P	P21	O	Functional Timer2 output.	Positive
	FTM2N	P22	O	Functional Timer2 output.	Negative
	FTM3P	P26	O	Functional Timer3 output.	Positive
	FTM3N	P27	O	Functional Timer3 output.	Negative
	EXTRG0	P02	I	Functional Timer0-3 event trigger input pin.	—
	EXTRG1	P03	I	Functional Timer0-3 event trigger input pin.	—
	EXTRG2	P04	I	Functional Timer0-3 event trigger input pin.	—
	EXTRG3	P17	I	Functional Timer0-3 event trigger input pin.	—
	EXTRG4	P21	I	Functional Timer0-3 event trigger input pin.	—
	EXTRG5	P23	I	Functional Timer0-3 event trigger input pin.	—
	EXTRG6	P26	I	Functional Timer0-3 event trigger input pin.	—
	EXTRG7	P27	I	Functional Timer0-3 event trigger input pin.	—
16bit General Timer	TMH0OUT	P04	O	16bit General Timer 0 output pin	Positive
	TMH1OUT	P13	O	16bit General Timer 1 output pin	Positive
	TMH2OUT	P23	O	16bit General Timer 2 output pin	Positive
	TMH3OUT	P13 P33	O	16bit General Timer 3 output pin	Positive
	TMH4OUT	P12	O	16bit General Timer 4 output pin	Positive
	TMH5OUT	P16	O	16bit General Timer 5 output pin	Positive
Time Base Counter (TBC)	TBCOUT1	P20	O	Time Base Counter 1Hz/2Hz output pin	Positive
		P27			
Buzzer	BZ0P	P17	O	Buzzer output (positive phase)	Positive
		P26			
	BZ0N	P20	O	Buzzer output (negative phase)	Negative
		P27			

Table 4 Pin Description (4/4)

Function	Signal name	Pin name	I/O	Description	Logic
External Interrupt	EXI0	P02	I	GPIO maskable external interrupt pin	—
	EXI1	P03	I	GPIO maskable external interrupt pin	—
	EXI2	P04	I	GPIO maskable external interrupt pin	—
	EXI3	P17	I	GPIO maskable external interrupt pin	—
	EXI4	P21	I	GPIO maskable external interrupt pin	—
	EXI5	P23	I	GPIO maskable external interrupt pin	—
	EXI6	P26	I	GPIO maskable external interrupt pin	—
	EXI7	P27	I	GPIO maskable external interrupt pin	—
Successive approximation type A/D converter	V _{REF}	P23	—	SA type A/D converter external reference voltage input. The voltage provided to the pin is used as the reference voltage for the A/D conversion.	—
	AIN0	P17	I	SA type A/D converter channel 0 input pin	—
	AIN1	P20	I	SA type A/D converter channel 1 input pin	—
	AIN2	P21	I	SA type A/D converter channel 2 input pin	—
	AIN3	P22	I	SA type A/D converter channel 3 input pin	—
	AIN4	P24	I	SA type A/D converter channel 4 input pin	—
	AIN5	P25	I	SA type A/D converter channel 5 input pin	—
	AIN6	P26	I	SA type A/D converter channel 6 input pin	—
	AIN7	P27	I	SA type A/D converter channel 7 input pin	—
Analog comparator	CMP0P	P03	I	Comparator input 0 (noninverting input)	—
	CMP0M	P02	I	Comparator input 0 (inverting input)	—
D/A converter	DACOUT	P01	O	D/A converter0 output pin	—

TERMINATION OF UNUSED PINS

Table 5 Termination of unused pins

Pin	Recommended pin termination
RESET_N	Connect to V_{DD} through a resistor
P00/TEST0	Open the pin with the internal initial condition of pulled-up input mode.
P01 to P07	Open the pins with the internal initial condition of Hi-impedance mode.
P10 to P17	
P20 to P27	
P30 to P33	

Note:

For unused input ports or unused input/output ports, if an unstable middle level voltage is supplied to the corresponding pins which are configured as inputs without pull-up register or input/output mode, supply current may become excessively large. Therefore, it is recommended to configure those pins as either input mode with a pull-up resistor or output mode.

ELECTRICAL CHARACTERISTICS (T.B.D.)

Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V _{DD}	Ta = +25°C	-0.3 to +6.5	V
Power supply voltage 2	V _{DDL}	Ta = +25°C	-0.3 to +2.0	V
Input voltage	V _{IN}	Ta = +25°C	-0.3 to V _{DD} +0.3 ^{*1}	V
Output voltage1	V _{OUT1}	Ta = +25°C	-0.3 to V _{DD} +0.3 ^{*1}	V
Output voltage2	V _{OUT2}	Ta = +25°C	-0.3 to +6.5	V
“H” level output current	I _{OUTH}	Ta = +25°C	1pin	mA
			Total	
“L” level output current	I _{OUTL}	Ta = +25°C	1pin	mA
			Total	
Power dissipation	PD	Ta = +25°C	1	W
Storage temperature	T _{STG}	—	-55 to +150	°C

^{*1} 6.5V or lower^{*2} The current flowing out the LSI through the pin is described in the negative number.

The applicable maximum current is the absolute value.

For example, -1mA means the maximum current 1mA flows out the LSI through the pin.

[Note] Use the product within absolute maximum ratings. The absolute maximum ratings are conditions which may physically deteriorate the quality of product.

Recommended Operating Conditions

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T _{OP}	—	-40 to +105	°C
Operating voltage 1	V _{DD}	—	1.6 to 5.5	V
Operating frequency (CPU)	f _{OP}	V _{DD} = 1.6 to 5.5V	30k to 4M	Hz
		V _{DD} = 1.8 to 5.5V	30k to 25M	
V _{DDL} pin external capacitance	C _L	—	1.0 ±30%	μF

Current Consumption

(V_{DD}=1.6 to 5.5V, V_{SS}=0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ. * ³	Max.	Unit	Measuring circuit
Supply current 0	IDD0	CPU is in STOP-D state. Low-speed RC1K/RC32K and PLL oscillation are stopped.	Ta = -40 to +85 °C	—	0.60 (TBD)	(TBD)	μA	1
			Ta = -40 to +105 °C	—		(TBD)		
Supply current 1	IDD1	CPU is in STOP state. Low-speed RC1K/RC32K and PLL oscillation are stopped.	Ta = -40 to +85 °C	—	0.80 (TBD)	(TBD)	μA	
			Ta = -40 to +105 °C	—		(TBD)		
Supply current 2	IDD2	Internal RC Oscillating. CPU is in HALT state (LTBC and WDT are operating ^{*1}). PLL oscillation is stopped.	Ta = -40 to +85 °C	—	5.0 (TBD)	(TBD)	μA	
			Ta = -40 to +105 °C	—		(TBD)		
Supply current 3	IDD3	CPU: Running with 32kHz RC oscillation clock ^{*1*} ^{*2} PLL oscillation is stopped.	Ta = -40 to +105 °C	—	18 (TBD)	(TBD)	μA	
Supply current 4	IDD4	CPU: Running with 16MHz PLL oscillating clock ^{*2} PLL 32MHz is oscillating. V _{DD} =1.8~5.5V	Ta = -40 to +105 °C	—	6.5 (TBD)	(TBD)	mA	
Supply current 5	IDD5	CPU: Running with 24MHz PLL oscillating clock ^{*2} PLL 24MHz is oscillating. V _{DD} =1.8~5.5V	Ta = -40 to +105 °C	—	7.5 (TBD)	(TBD)		

*¹ LTBC and WDT is operating, Significant bits of BLKCON0-3 and BRECON0-3 registers are all "1"*² CPU running in wait mode*³ On the condition of V_{DD}=3.0V, Ta=+25° C

On-chip Oscillator

(V_{DD}=1.6 to 5.5V, V_{SS}=0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Low-speed RC oscillator frequency accuracy 1	f _{RCL1}	Ta= +25°C V _{DD} = 1.8 to 5.5V Without software adjustment * ¹	Typ -1.0%	32.768	Typ +1.0%	kHz	1
		Ta= -40 to +85°C V _{DD} = 1.8 to 5.5V Without software adjustment * ¹	Typ -2.5%	32.768	Typ +2.5%		
		Ta= -40 to +105°C V _{DD} = 1.8 to 5.5V Without software adjustment * ¹	Typ -3.0%	32.768	Typ +3.0%		
		V _{DD} = 1.6 to 1.8V Without software adjustment * ¹	Typ -3.5%	32.768	Typ -3.5%		
Low-speed RC oscillator frequency accuracy 2	f _{RCL2}	Ta= -40 to +85°C V _{DD} = 1.8 to 5.5V With software adjustment * ¹	Typ -1.0%	32.768	Typ +1.0%		
		Ta= -40 to +105°C V _{DD} = 1.8 to 5.5V With software adjustment * ¹	Typ -1.5%	32.768	Typ +1.5%		
PLL oscillation frequency accuracy 1	f _{PLL1}	Ta= -40 to +85°C V _{DD} = 1.8 to 5.5V Without software adjustment * ¹	Typ -2.5%	16/24	Typ +2.5%	MHz	
		Ta= -40 to +105°C V _{DD} = 1.8 to 5.5V Without software adjustment * ¹	Typ -3.0%	16/24	Typ +3.0%		
		V _{DD} = 1.6 to 1.8V Without software adjustment * ¹	Typ -3.5%	16/24	Typ +3.5%		
PLL oscillation frequency accuracy 2	f _{PLL2}	Ta= -40 to +85°C V _{DD} = 1.8 to 5.5V With software adjustment * ¹	Typ -1.0%	16/24	Typ +1.0%		
		Ta= -40 to +105°C V _{DD} = 1.8 to 5.5V With software adjustment * ¹	Typ -1.5%	16/24	Typ +1.5%		
PLL oscillation start time	T _{PLL}	V _{DD} = 1.6 to 5.5V	—	—	2	ms	
1kHz Low-speed RC oscillator (for WDT) frequency accuracy	f _{RC1K}	Ta= -40 to +105°C V _{DD} = 1.6 to 5.5V	0.5	1	2.5	kHz	

^{*1} Adjust the frequency by using temperature sensor in ADC and a Specific Function Register (LRCADJ register)

Input / Output pin 1

(V_{DD}=1.6 to 5.5V, V_{SS}=0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
Output voltage1 “H”/“L” level (P00-P07) (P10-P17) (P20-P27) (P30-P33)	VOH1	IOH1=-1mA		V _{DD} -0.5	—	—	V	2
	VOL1	IOL1=+1mA		—	—	0.5		
Output voltage2 “L” level (P01-P07) (P10-P17) (P20-P27) (P30-P33)	VOL2	When Nch open drain output mode is selected	IOL2=+10mA V _{DD} ≥5.0V	—	—	0.5		
			IOL2=+8mA V _{DD} ≥3.0V	—	—	0.5		
			IOL2=+3mA V _{DD} ≥2.0V	—	—	0.4		
			IOL2=+2mA 2.0V>V _{DD} ≥1.6V	—	—	0.4		

Input / Output pin 2

(V_{DD}=1.6 to 5.5V, V_{SS}=0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
“H” level output current1 ^{*1}	IOH1	1pin VOH≥V _{DD} -0.5		-1 ^{*3*5}	—	—	mA	3
		Total of ‘P00-P07, P10-P13		-10 ^{*5}	—	—		
		Total of ‘P14-P17, P20-P27, P30-P33		-10 ^{*5}	—	—		
		All pin total		-20 ^{*5}	—	—		
“L” level output current1 ^{*2}	IOL1	1pin (CMOS output mode)		—	—	1 ^{*3}		
“L” level output current2 ^{*2}	IOL2	1pin (Nch open drain output mode)		—	—	10 ^{*3}		
“L” level output total current ^{*2*4}	IOL3	Total of P00-P07, P10-P13, (Nch open drain output mode,duty≤50%)	V _{DD} ≥5.0V	—	—	60		
			V _{DD} ≥3.0V	—	—	40		
			V _{DD} ≥2.0V	—	—	15		
			2.0V>V _{DD} ≥1.6V	—	—	10		
		Total of P14-P17, P20-P27,P30-P33 (Nch open drain output mode,duty≤50%)	V _{DD} ≥5.0V	—	—	60		
			V _{DD} ≥3.0V	—	—	40		
			V _{DD} ≥2.0V	—	—	15		
			2.0V>V _{DD} ≥1.6V	—	—	10		
		All pin total (Nch open drain output mode,duty≤50%)		—	—	120		
Output leak (P01-P07) (P10-P17) (P20-P27) (P30-P33)	IOOH	VOH=V _{DD} (High impedance mode)		—	—	+1	μA	
	IOOL	VOL=V _{SS} (High impedance mode)		-1 ^{*5}	—	—		

^{*1} Sink-out current from V_{DD} to the output pin, which can guarantee the device operation.

^{*2} Sink-in current from the output pin to V_{SS}, which can guarantee the device operation.

^{*3} Do not exceed total current.

^{*4} The total current is on the condition of Duty ≤ 50% (same applies to IOH1).

When the duty > 50% the total current is calculated by following formula.

Total current = IOL3 × 50/n (When the duty is n%)

<For an example> When IOL3=100mA and n=80%,

Total current = IOL3 × 50/80 = 62.5mA

Current allowed per 1pin is independent of the duty and specified as IOL1 and IOL2.

Do not apply current larger than Absolute Maximum Ratings.

^{*5} The current flowing out the LSI through the pin is described in the negative number.

The applicable maximum current is the absolute value.

For example, -1mA means the maximum current 1mA flows out the LSI through the pin.

(V_{DD}=1.6 to 5.5V, V_{SS}=0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Input current1 (RESET_N)	I _{IH1}	V _{IH1} =V _{DD}	—	—	1	μA	4
	I _{IL1}	V _{IL1} =V _{SS}	-1* ¹	—	—		
Input current2 (P00/TEST0)	I _{IL2}	V _{IL2} =V _{SS} (pull-up mode)	-1500* ¹	-300* ¹	-20* ¹	kΩ	
	V/I _{IL2}	V _{IL2} =V _{SS} (pull-up mode)	3.7	10	80	μA	
	I _{IH2Z}	V _{IH2} =V _{DD} (High impedance mode)	—	—	1		
	I _{IL2Z}	V _{IL2} =V _{SS} (High impedance mode)	-1* ¹	—	—		
Input current3 (P01-P07) (P10-P17) (P20-P27) (P30-P33)	I _{IL3}	V _{IL3} =V _{SS} (pull-up mode)	-250* ¹	-30* ¹	-2* ¹	kΩ	
	V/I _{IL3}	V _{IL3} =V _{SS} (pull-up mode)	22	100	800		
	I _{IH3Z}	V _{IH3} =V _{DD} (High impedance mode)	—	—	1	μA	
	I _{IL3Z}	V _{IL3} =V _{SS} (High impedance mode)	-1* ¹	—	—		
Input voltage1 (RESET_N) (P00/TEST0) (P01-P07) (P10-P17) (P20-P27) (P30-P33)	V _{IH1}	—	0.7 x V _{DD}	—	V _{DD}	V	5
	V _{IL1}	—	0	—	0.3 x V _{DD}		
Pin capacitance (RESET_N) (P00/TEST0) (P01-P07) (P10-P17) (P20-P27) (P30-P33)	C _{PIN}	f = 10kHz Ta = +25°C	—	—	10	pF	—

^{*1} The current flowing out the LSI through the pin is described in the negative number.

The applicable maximum current is the absolute value.

For example, -1mA means the maximum current 1mA flows out the LSI through the pin.

Synchronous Serial Port

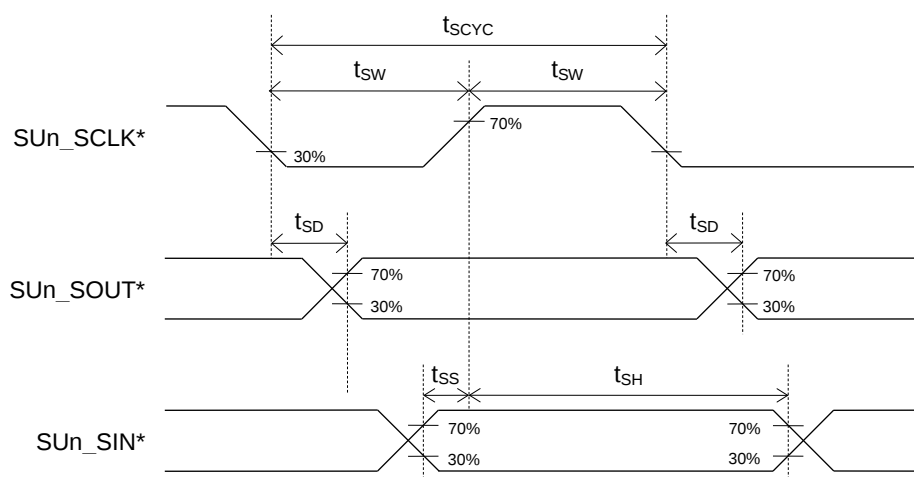
Slave mode

(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCK input cycle	t _{SCYC}	—	1 * ²	—	—	μs
SCK input pulse width	t _{SW}	—	0.5 * ³	—	—	μs
SOUT output delay time	t _{SD}	V _{DD} =2.4 to 5.5V	—	—	100+ HCLK* ¹ ×3	ns
		V _{DD} =1.8 to 5.5V	—	—	200+ HCLK* ¹ ×3	ns
SIN input setup time	t _{SS}	—	HCLK* ¹ x1	—	—	ns
SIN input hold time	t _{SH}	—	80+ HCLK* ¹ ×3	—	—	ns

*¹ Cycle of high speed clock

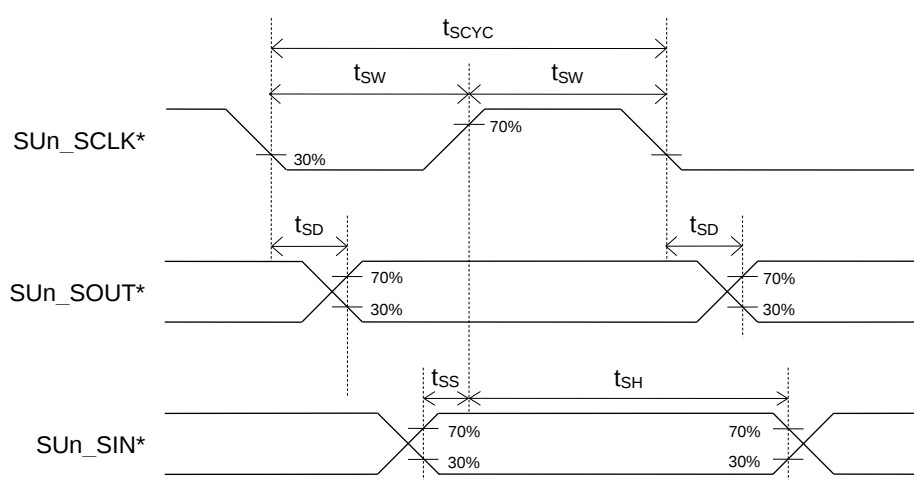
*² Need input cycles of HSLCK x8 or longer

*³ Need input cycles of HSLCK x4 or longer

* 2nd to 8th function of port, n=0~1

Master mode

(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCK output cycle	t _{SCYC}	—	—	SCLK* ¹	—	ns
SCK output pulse width	t _{SW}	—	SCLK* ¹ ×0.4	SCLK* ¹ ×0.5	SCLK* ¹ ×0.6	ns
SOUT output delay time	t _{SD}	V _{DD} =2.4 to 5.5V	—	—	100	ns
		V _{DD} =1.8 to 5.5V	—	—	160	ns
SIN input setup time	t _{SS}	V _{DD} =2.4 to 5.5V	120	—	—	ns
		V _{DD} =1.8 to 5.5V	180	—	—	ns
SIN input hold time	t _{SH}	V _{DD} =2.4 to 5.5V	80	—	—	ns
		V _{DD} =1.8 to 5.5V	100	—	—	ns

¹ Clock cycle selected by bit12~8(SnCK4~0) of the serial port n mode register (SIO_nMOD)V_{DD}≥2.4V: min250ns, V_{DD}≥1.8V: min500ns 2nd to 8th function of port, n=0~1

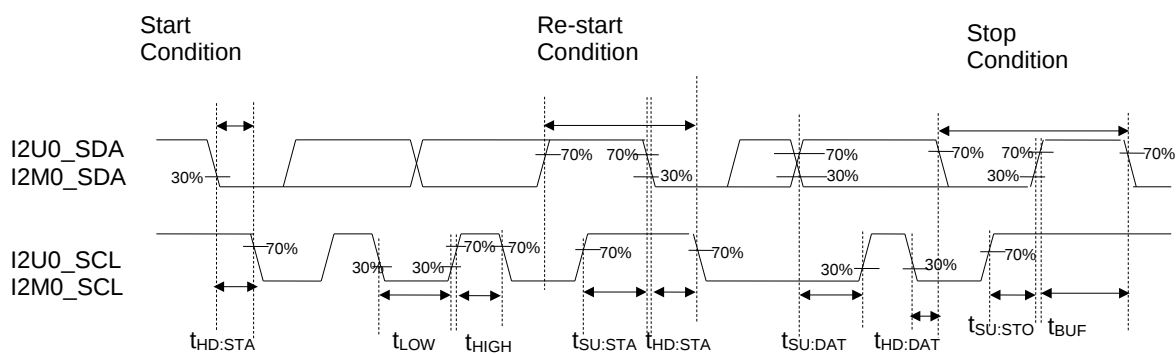
I²C Bus Interface

Standard Mode 100kHz

(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f _{SCL}	—	0	—	100	kHz
SCL hold time (start/restart condition)	t _{HD:STA}	—	4.0	—	—	μs
SCL "L" level time	t _{LOW}	—	4.7	—	—	μs
SCL "H" level time	t _{HIGH}	—	4.0	—	—	μs
SCL setup time (restart condition)	t _{SU:STA}	—	4.7	—	—	μs
SDA hold time	t _{HD:DAT}	—	0	—	—	μs
SDA setup time	t _{SU:DAT}	—	0.25	—	—	μs
SDA setup time (stop condition)	t _{SU:STO}	—	4.0	—	—	μs
Bus-free time	t _{BUF}	—	4.7	—	—	μs

When using the I²C as the master, configure the I²C master n mode register(I2MnMOD) and I²C bus 0 mode register (master side, I2UM0MOD) so that meet these specifications.

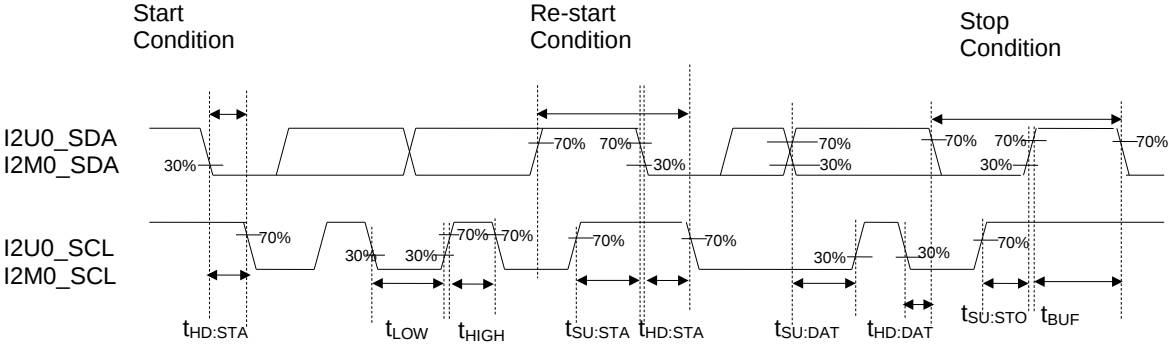


Fast Mode 400kHz

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f _{SCL}	—	0	—	400	kHz
SCL hold time (start/restart condition)	t _{HD:STA}	—	0.6	—	—	μs
SCL "L" level time	t _{LOW}	—	1.3	—	—	μs
SCL "H" level time	t _{HIGH}	—	0.6	—	—	μs
SCL setup time (restart condition)	t _{SU:STA}	—	0.6	—	—	μs
SDA hold time	t _{HD:DAT}	—	0	—	—	μs
SDA setup time	t _{SU:DAT}	—	0.1	—	—	μs
SDA setup time (stop condition)	t _{SU:STO}	—	0.6	—	—	μs
Bus-free time	t _{BUF}	—	1.3	—	—	μs

When using the I²C as the master, configure the I²C master n mode register(I2MnMOD) and I²C bus 0 mode register (master side, I2UM0MOD) so that meet these specifications.

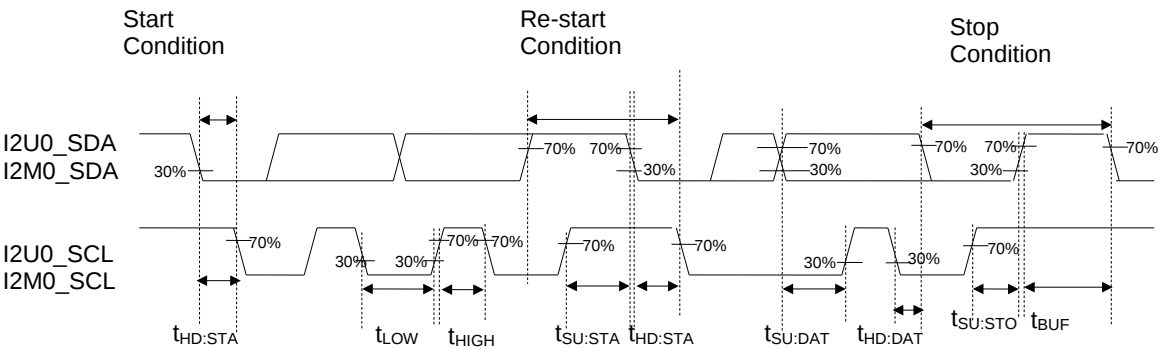


1Mbps Mode

(V_{DD}=2.7 to 5.5V, V_{SS} =0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCL clock frequency	f _{SCL}	—	0	—	1000	kHz
SCL hold time (start/restart condition)	t _{HD:STA}	—	0.26	—	—	μs
SCL "L" level time	t _{LOW}	—	0.5	—	—	μs
SCL "H" level time	t _{HIGH}	—	0.26	—	—	μs
SCL setup time (restart condition)	t _{SU:STA}	—	0.26	—	—	μs
SDA hold time	t _{HD:DAT}	—	0	—	—	μs
SDA setup time	t _{SU:DAT}	—	0.1	—	—	μs
SDA setup time (stop condition)	t _{SU:STO}	—	0.26	—	—	μs
Bus-free time	t _{BUF}	—	0.5	—	—	μs

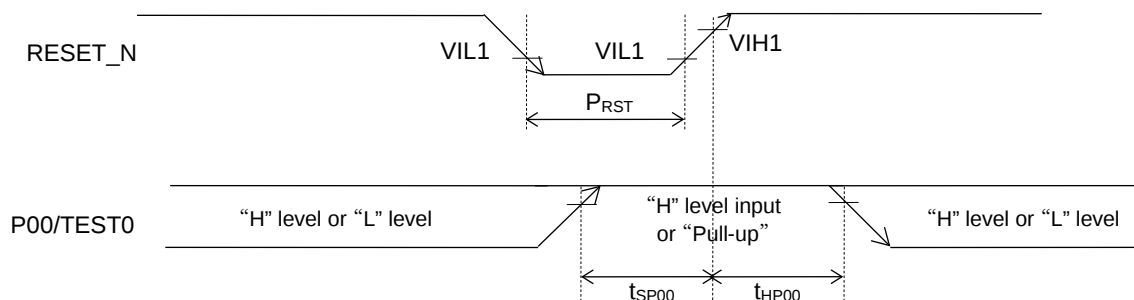
When using the I²C as the master, configure the I²C master n mode register(I2MnMOD) and I²C bus 0 mode register (master side, I2UM0MOD) so that meet these specifications.



Reset

(V_{DD}=1.6 to 5.5V, V_{SS}=0V, Ta=-40 to +105°C, unless otherwise specified)

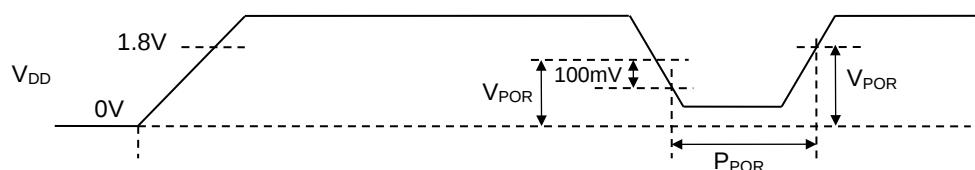
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Reset pulse width	P _{RST}	—	2	—	—	ms	1
P00 "H" level setup time	t _{SP00}	—	1	—	—	ms	
P00 "H" level hold time	t _{HP00}	—	1	—	—	ms	



Power On Reset

(V_{SS}=0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
POR detect voltage	V _{POR}	Power down(falling)	1.40	1.46	1.58	V	1
		Power up(rising)	1.39	1.49	1.8	V	
Power on rising slope	R _{POR} * ¹	—	—	—	60	V/ms	
POR response time	P _{POR}	* ²	200	—	—	μs	

*¹: Rise the V_{DD} to 1.8V or higher when powering on.*²: This is the time from the V_{DD} gets 100mV lower than V_{POR} to the Power-On-Reset internally generates.
Make the power down falling slope 2V/ms or lower(i.e. slower).

[Note for in case of instantaneous power failure]

In case of instantaneous power failure and a pulse shorter than the response time of VLS or POR is asserted to V_{DD}, it is possible to make the MCU cannot get the reset and make erroneous operation. In that case, please have countermeasures such as preventing the voltage down using bypass capacitor or making reset pin reset.

VLS

(V_{DD}=1.6 to 5.5V, V_{SS}=0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
		VLS0LV * ¹						
VLS threshold voltage * ²	V _{VLSR}	00H	Rising	3.86	4.06	4.26	V	1
	V _{VLSF}		Falling	3.84	4.00	4.16		
	V _{VLSR}	01H	Rising	3.57	3.76	3.95		
	V _{VLSF}		Falling	3.55	3.70	3.85		
	V _{VLSR}	02H	Rising	2.94	3.11	3.28		
	V _{VLSF}		Falling	2.92	3.05	3.18		
	V _{VLSR}	03H	Rising	2.85	3.01	3.17		
	V _{VLSF}		Falling	2.83	2.95	3.07		
	V _{VLSR}	04H	Rising	2.75	2.91	3.07		
	V _{VLSF}		Falling	2.73	2.85	2.97		
	V _{VLSR}	05H	Rising	2.66	2.81	2.96		
	V _{VLSF}		Falling	2.64	2.75	2.86		
	V _{VLSR}	06H	Rising	2.56	2.71	2.86		
	V _{VLSF}		Falling	2.54	2.65	2.76		
	V _{VLSR}	07H	Rising	2.46	2.61	2.76		
	V _{VLSF}		Falling	2.44	2.55	2.66		
	V _{VLSR}	08H	Rising	2.37	2.51	2.65		
	V _{VLSF}		Falling	2.35	2.45	2.55		
	V _{VLSR}	09H	Rising	1.98	2.11	2.24		
	V _{VLSF}		Falling	1.96	2.05	2.14		
	V _{VLSR}	0AH	Rising	1.89	2.01	2.13		
	V _{VLSF}		Falling	1.87	1.95	2.03		
	V _{VLSR}	0BH	Rising	1.79	1.91	2.03		
	V _{VLSF}		Falling	1.77	1.85	1.93		
VLS Current	I _{VLS}	—		—	50	—	nA	

^{*1} Bit3~Bit0 of voltage level detection circuit 0 level register (VLS0LV).^{*2} The Data VLS0LV = 0CH~0FH is not available to use, if the data is specified it will the same spec as that 0BH is specified.

Analog Comparator

(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Comparator same phase input voltage range	V _{CMR}	—	0.1	—	V _{DD} -1.5	V	1
Comparator0 input offset	V _{CMOF}	Ta=+25 °C, V _{DD} =5.0V	—	5	—	mV	
Comparator Reference Voltage	V _{CMREF}	—	0.75	0.8	0.85	V	

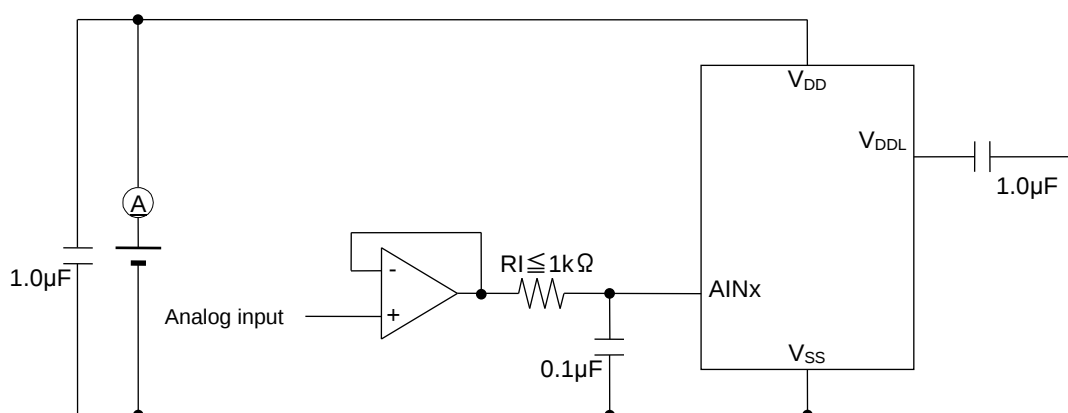
Successive Approximation Type A/D Converter

(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n _{AD}	—	—	—	10	bit
Integral non-linearity error	INL _{AD}	2.7V ≤ V _{REFP} ^{*1} ≤ 5.5V	-4	—	4	LSB
		2.2V ≤ V _{REFP} ^{*1} < 2.7V	-6	—	6	
		1.8V ≤ V _{REFP} ^{*1} < 2.2V	-10	—	10	
		V _{REFP} =Internal reference voltage	-15	—	15	
Differential non-linearity error	DNL _{AD}	2.7V ≤ V _{REFP} ^{*1} ≤ 5.5V	-3	—	3	
		2.2V ≤ V _{REFP} ^{*1} < 2.7V	-5	—	5	
		1.8V ≤ V _{REFP} ^{*1} < 2.2V	-9	—	9	
		V _{REFP} =Internal reference voltage	-14	—	14	
Zero-scale error	ZSE	RI ≤ 1kΩ	-6	—	6	V
Full-scale error	FSE	RI ≤ 1kΩ	-6	—	6	
A/D reference voltage	V _{REFX}	—	1.8	—	V _{DD}	
Internal reference voltage	V _{REFI}	—	1.5	1.55	1.6	μs
Conversion time	t _{CONV}	4.5V ≤ V _{DD} ≤ 5.5V	2.25	—	427	
		2.2V ≤ V _{DD} ≤ 5.5V	4.5	—	427	
		1.8V ≤ V _{DD} ≤ 5.5V	18	—	427	

^{*1} : V_{DD} or P23/V_{REF} is selected for the reference voltage of Successive Approximation Type A/D Converter by setting bit5(VREFP1) and bit4(VREFP0) of SA-ADC TEMP/VREF control register(VREFCON).

The current flows during the ADC sampling as it takes charging. Make the output impedance of the analog signal source 1kΩ or smaller. Also, putting 0.1μF capacitor on the ADC input pin is recommended to reduce the noise.



D/A Converter

(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n _{DA}	—	—	—	8	bit
Conversion cycle	tc	—	10	—	—	μs
Integral non-linearity error	INL _{DA}	RL=4MΩ	-2	—	2	LSB
Differential non-linearity error	DNL _{DA}	RL=4MΩ	-1	—	1	
Output impedance	R _o	DACEN bit of D/A converter enable register =1	3	6	9	kΩ

Reference Voltage Output

(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Output voltage	V _{REFOUT}	—	—	1.55	—	V
Output impedance	R _{VREFOUT}	—	—	—	500	kΩ

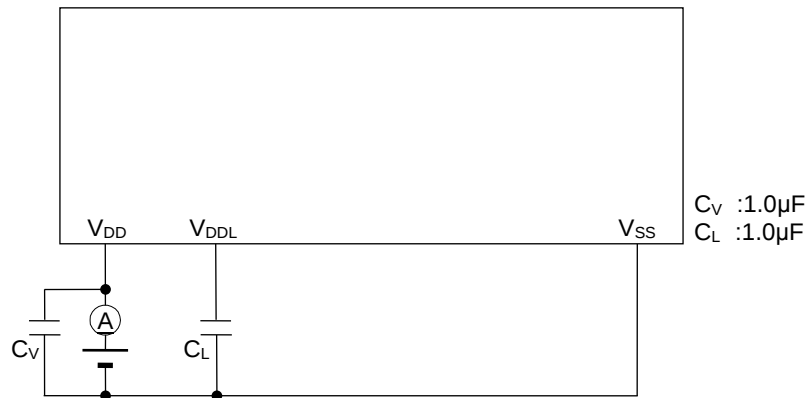
Flash Memory

(V_{SS}= 0V)

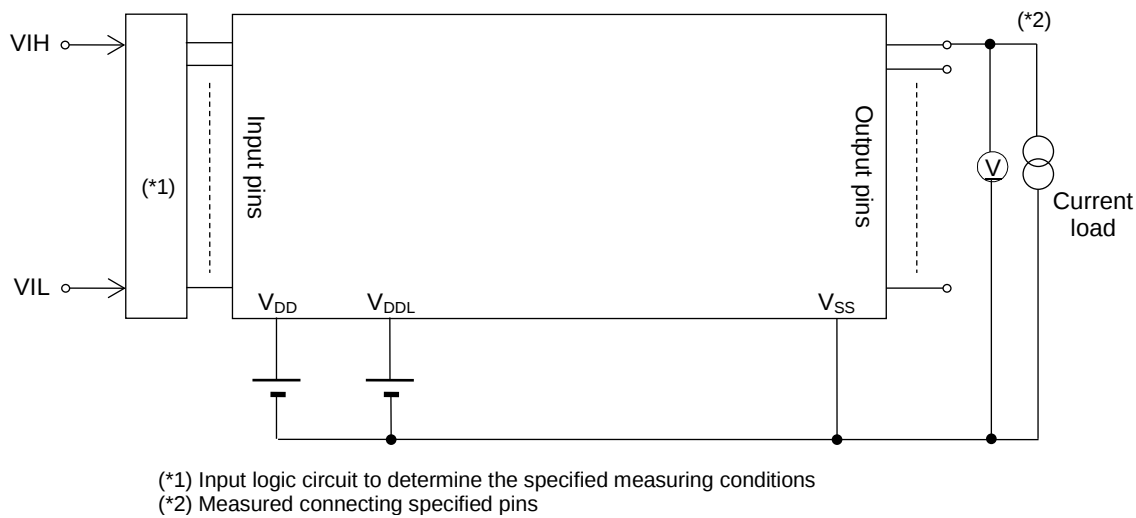
(V_{SS} = 0V)

Parameter	Symbol	Condition		Range	Unit
Operating temperature	T _{OP}	Data flash memory, At write/erase		-40 to +85	°C
		Flash ROM, At write/erase		0 to +40	
Operating voltage	V _{DD}	At write/erase		+1.8 to +5.5	V
Maximum rewrite count	CEPD	Data Flash (4Kbyte)		10000	times
	CEPP	Program Flash		100	
Erase unit	—	Block erase	Program Flash	16K	B
			Data Flash	2K	
	—	Sector erase	Program Flash	1K	B
			Data Flash	128	
Erase time (Max.)	—	Block erase / Sector erase		50	ms
Write unit	—	Program Flash		4	B
		Data Flash		1	
Write time (Max.)	—	Program Flash		80	μs
	—	Data Flash		40	
Data retention period	YDR	—		15	years

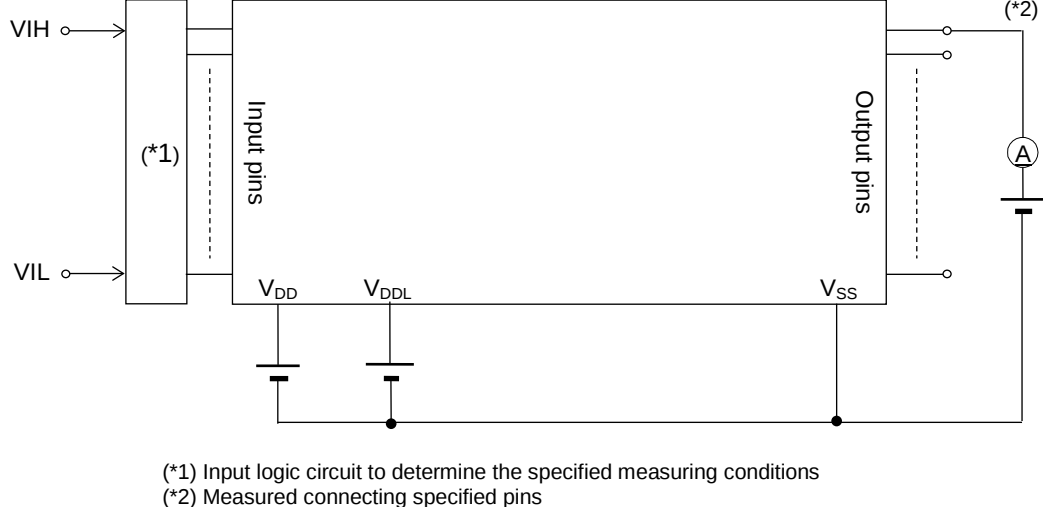
Measuring circuit 1



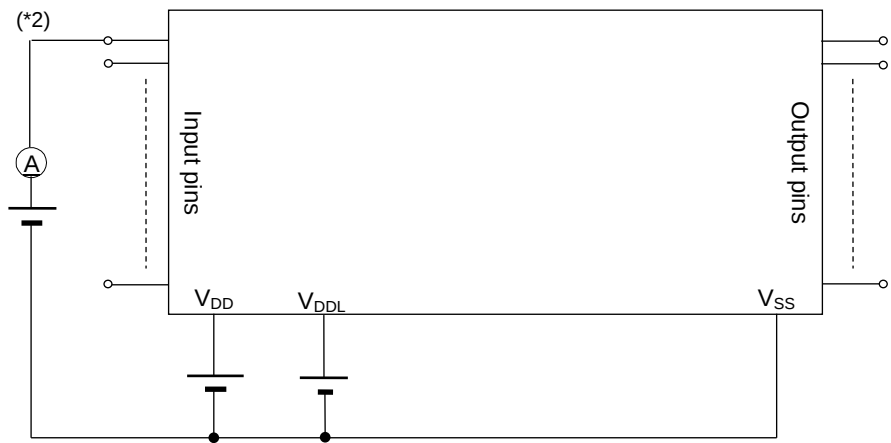
Measuring circuit 2



Measuring circuit 3

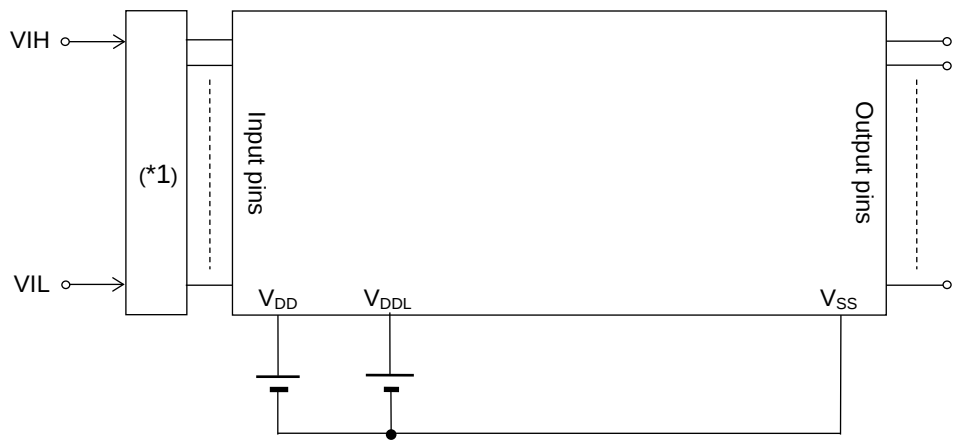


Measuring circuit 4



(*2) Measured connecting specified pins

Measuring circuit 5



(*1) Input logic circuit to determine the specified measuring conditions

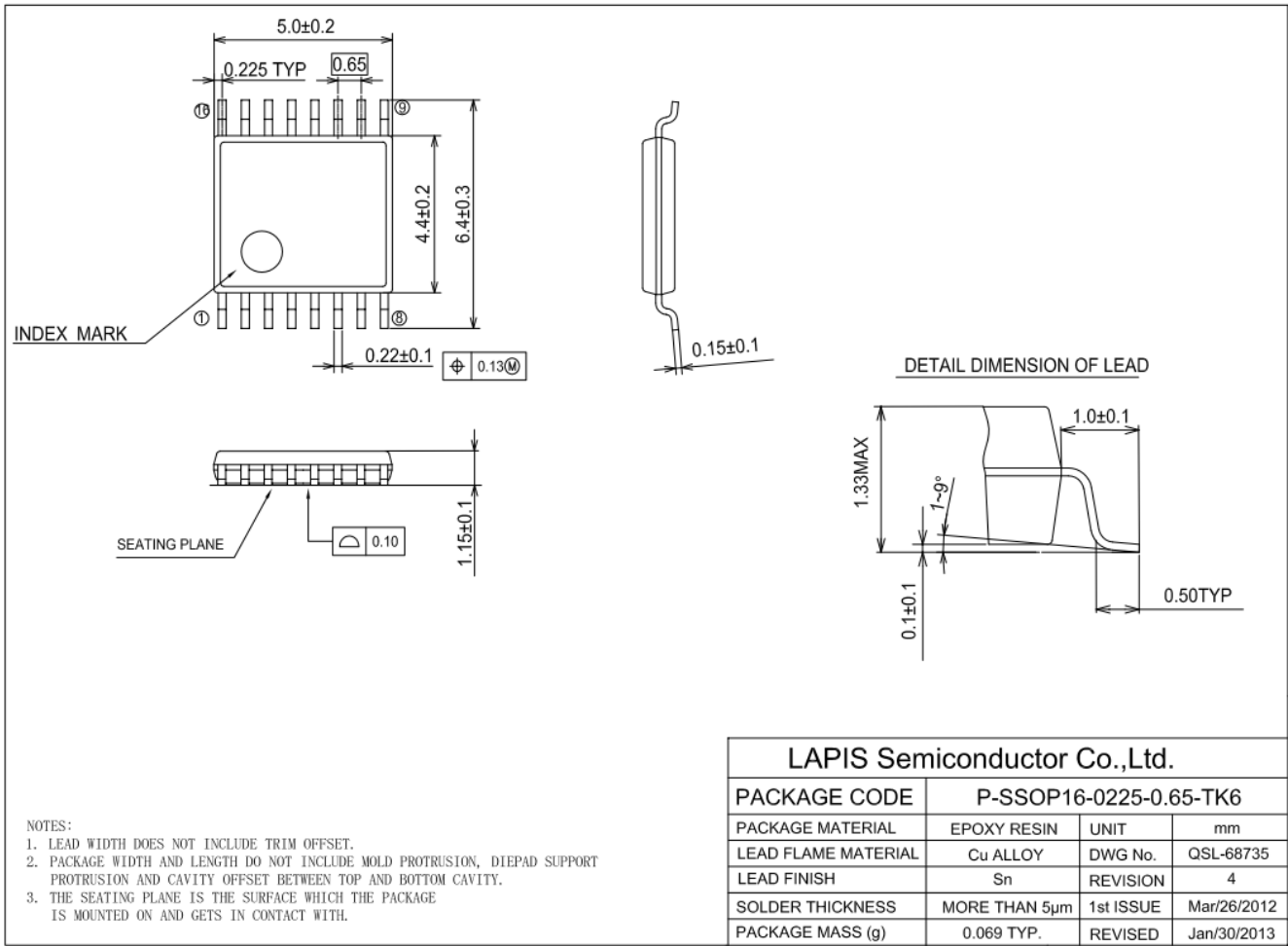
Characteristics graphs

These Graphs on the following pages are references for designing an application.

(T.B.D)

PACKAGE DIMENSIONS

ML62Q1323/1324/1325 16pin SSOP Package

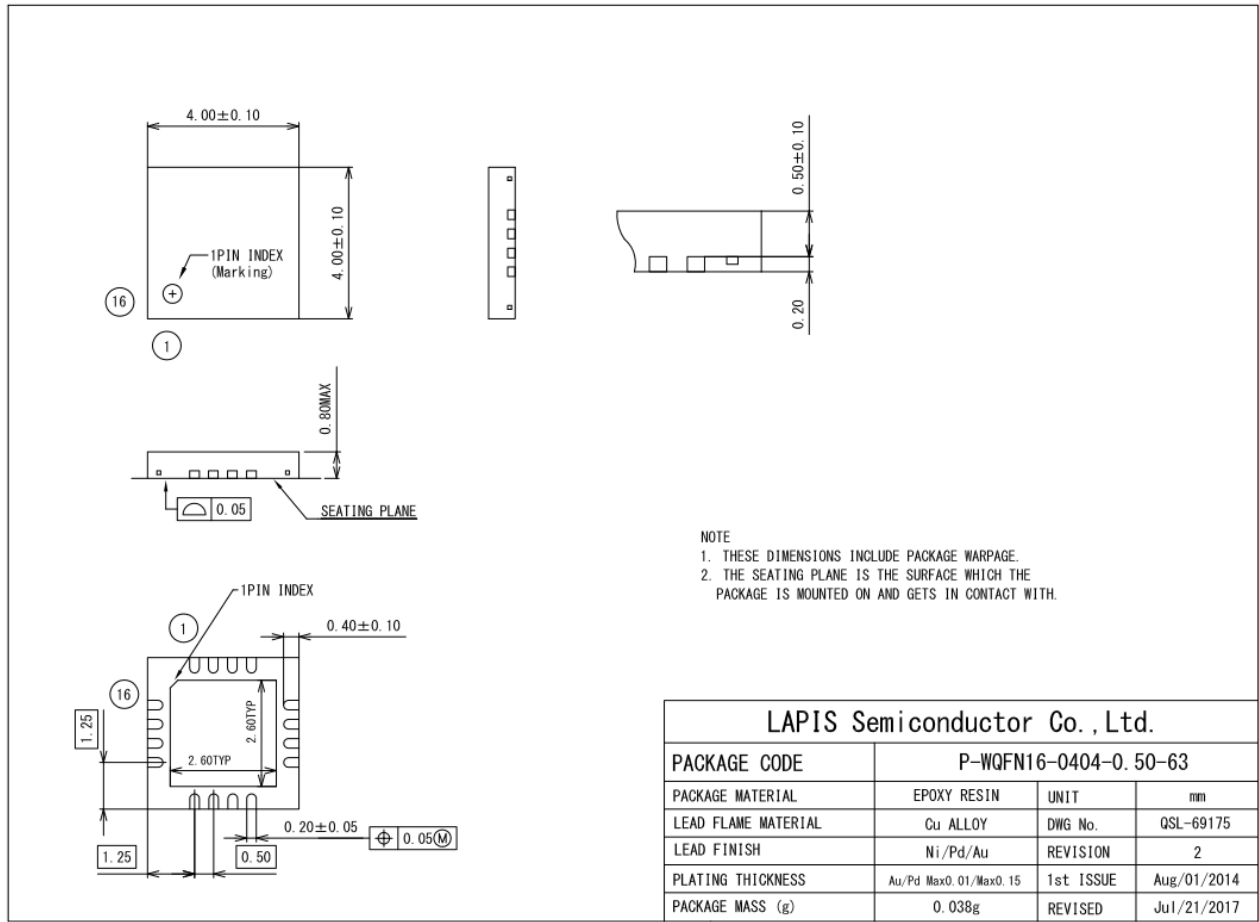


(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

ML62Q1323/1324/1325 16pin WQFN Package



(Unit: mm)

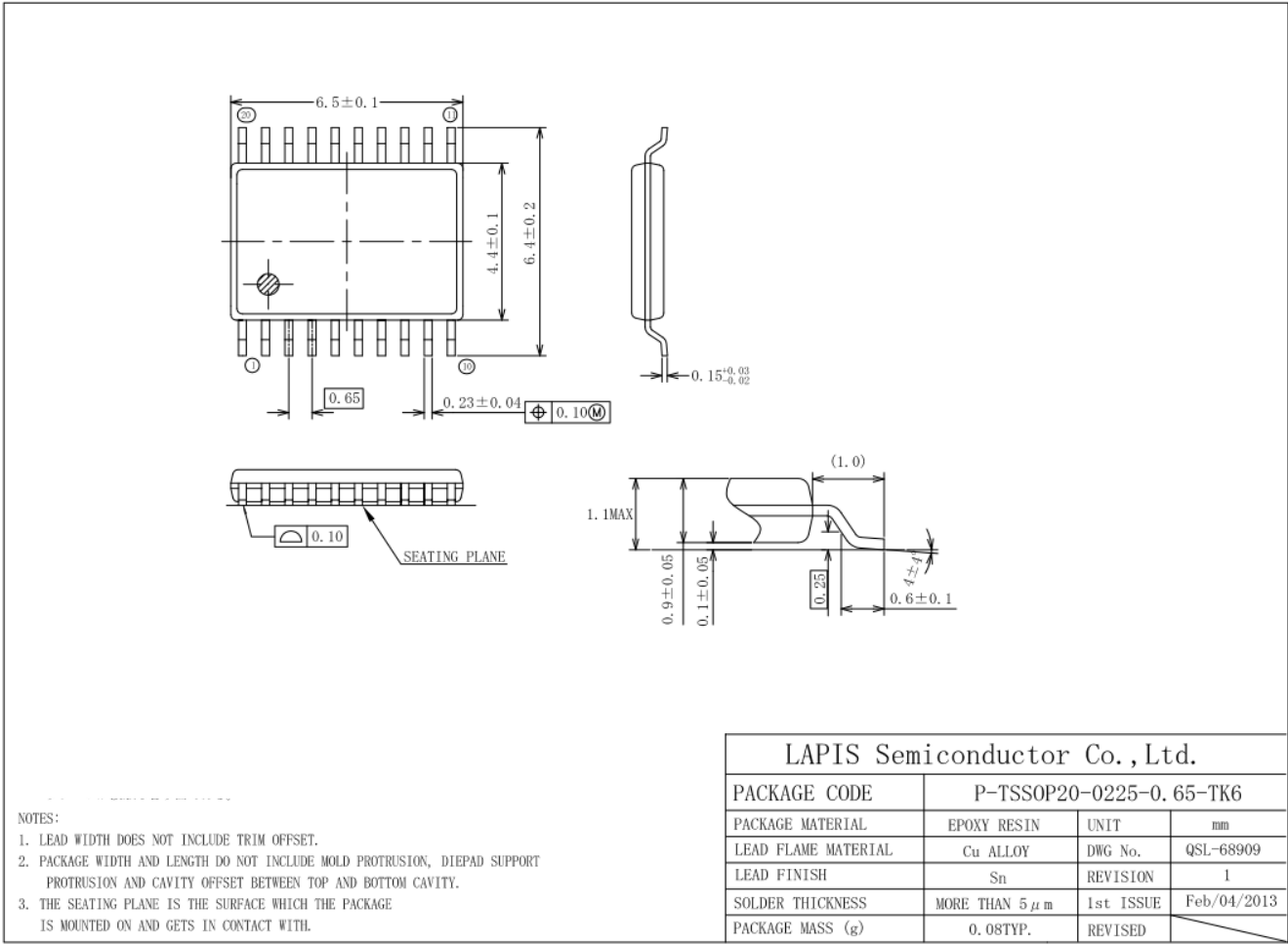
Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Note for the package with exposed die pad

The die pad is exposed on the bottom of WQFN package. Make the die pad electrically open when soldering onto the PCB.

ML62Q1333/1334/1335 20pin TSSOP Package

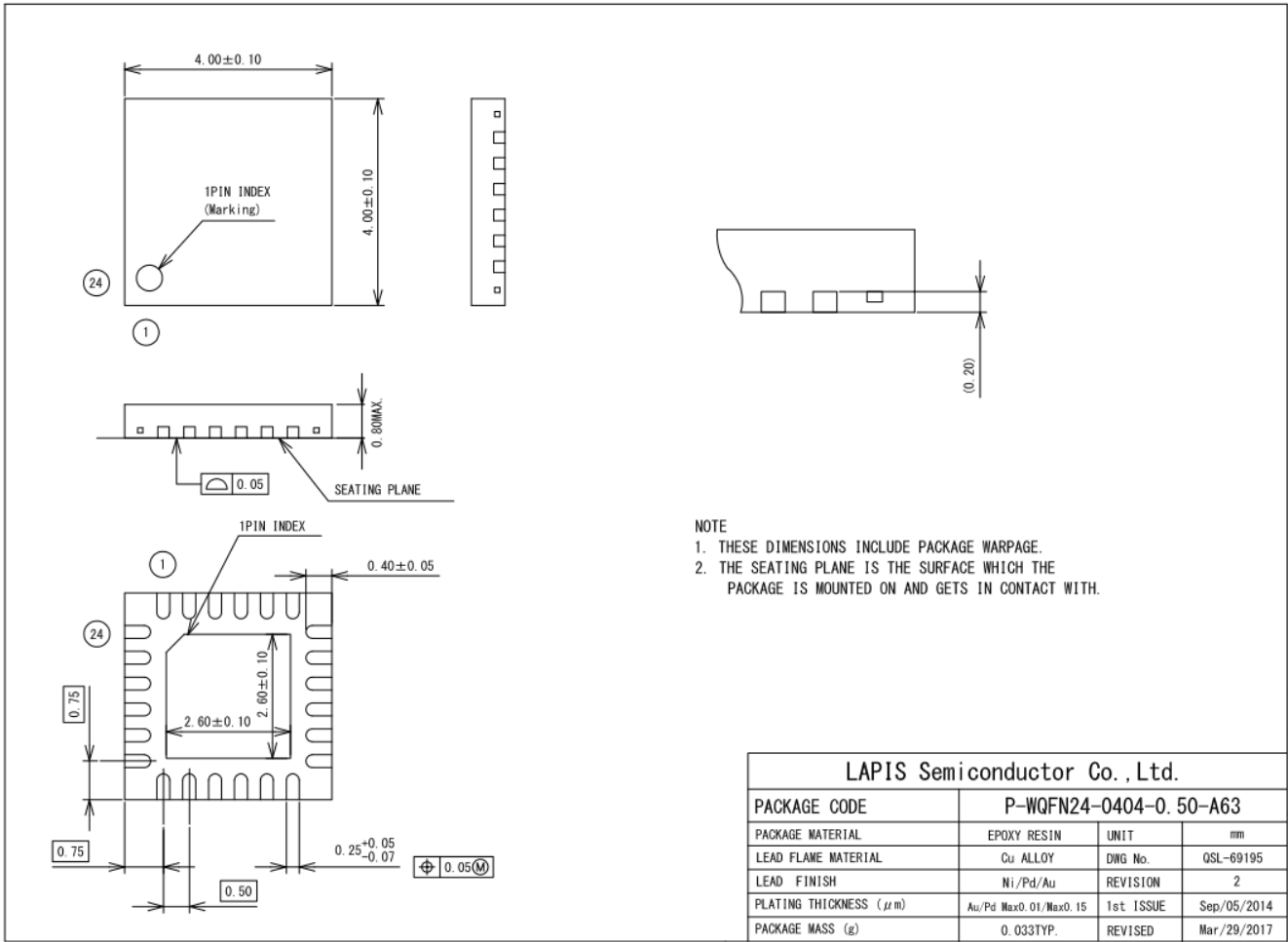


(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

ML62Q1345/1346/1347 24pin WQFN Package



(Unit: mm)

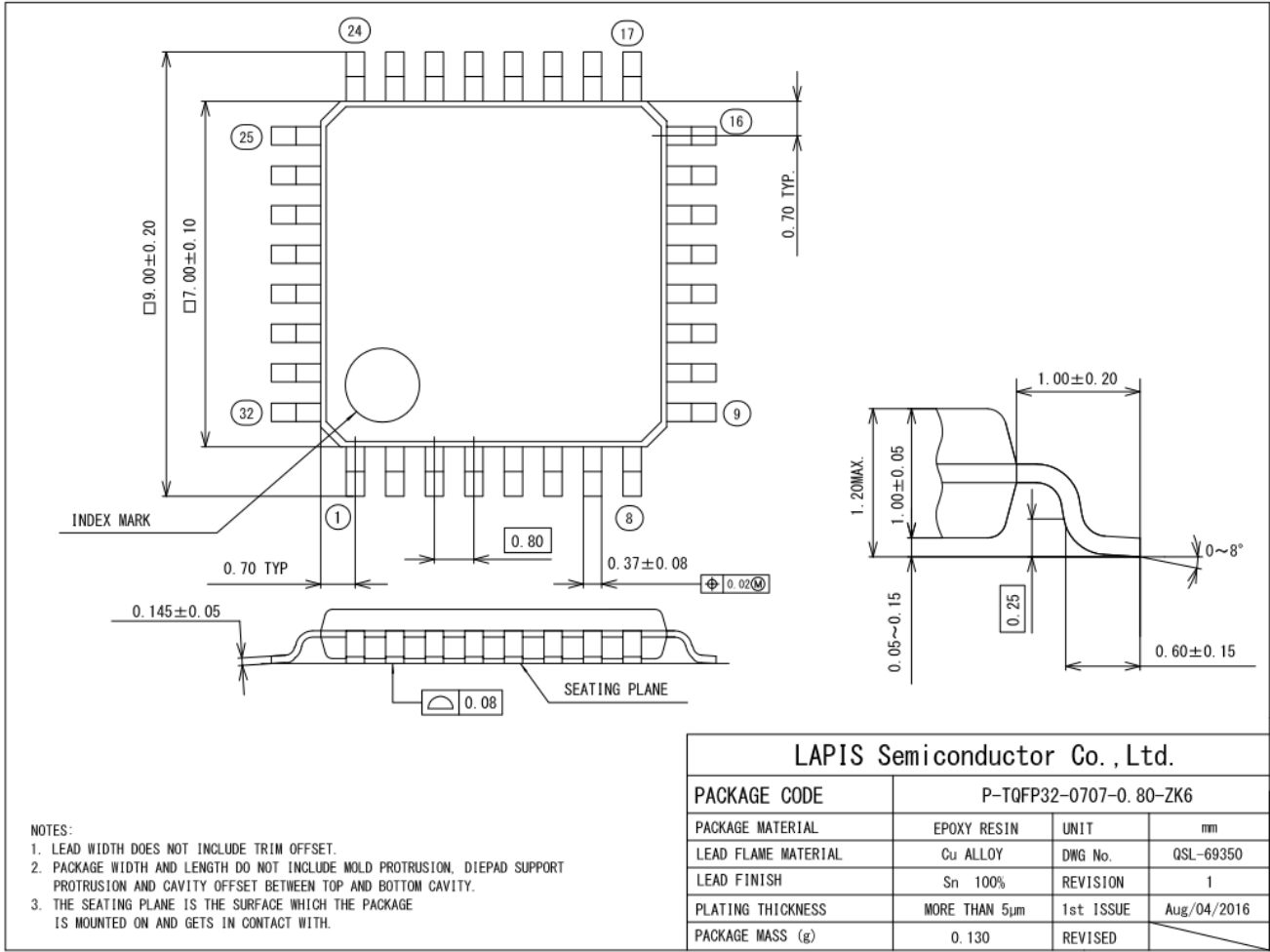
Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Note for the package with exposed die pad

The die pad is exposed on the bottom of WQFN package. Make the die pad electrically open when soldering onto the PCB.

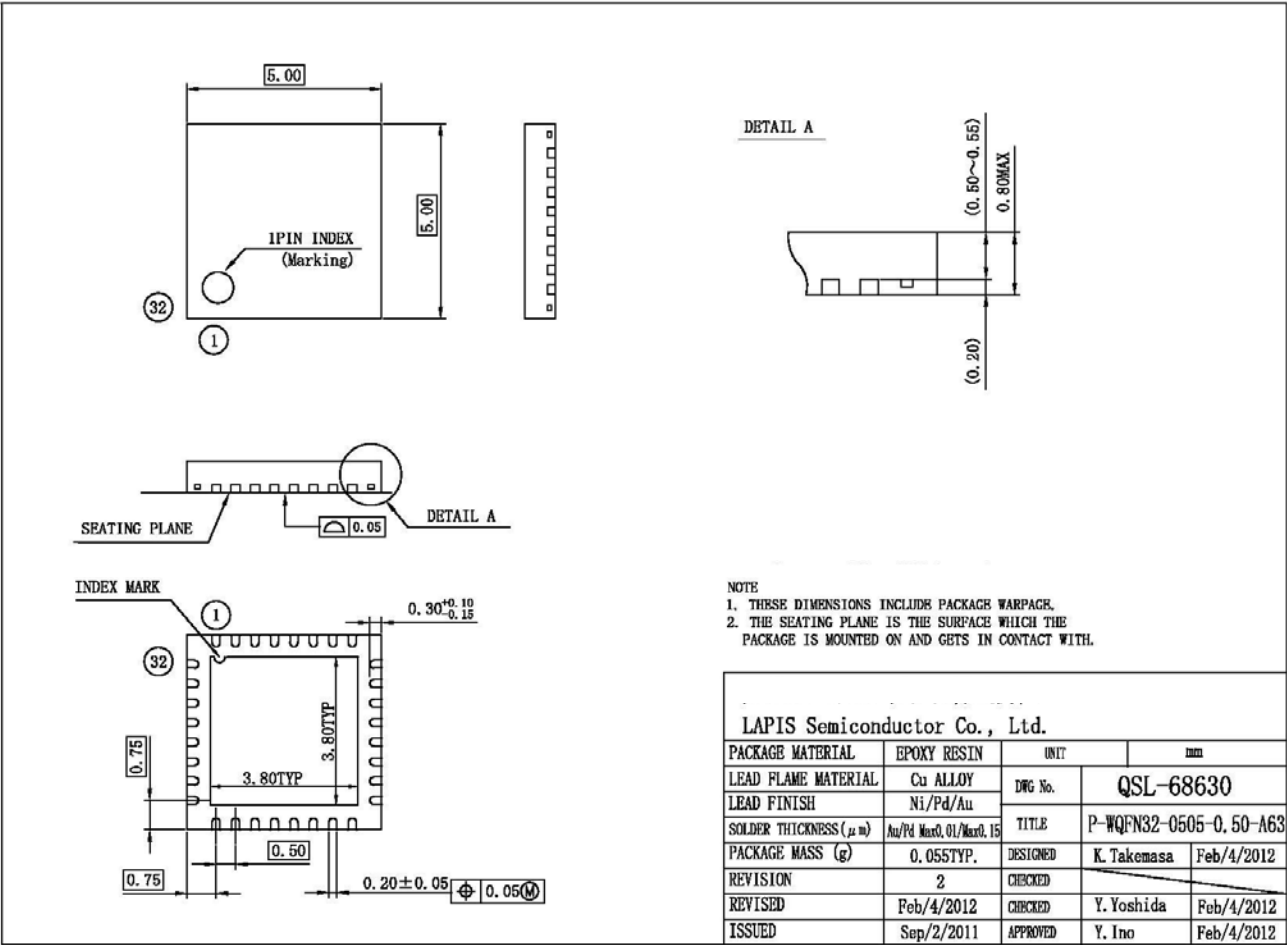
ML62Q1365/1366/1367 32pin TQFP Package



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

ML62Q1365/1366/1367 32pin WQFN Package



(Unit: mm)

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

Note for the package with exposed die pad

The die pad is exposed on the bottom of WQFN package. Make the die pad electrically open when soldering onto the PCB.

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL62Q1300-01	May 30, 2018	-	-	Preliminary 1 st Revision.
PEDL62Q1300-02	June 26, 2018	-	-	Add the package of WQFN32

Notes

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