for Wonderful Cruising
Safe + Comfortable Cabin

AK7739

Multi Core DSP with 4ch CODEC & SRC

1. General Description

The AK7739 is a highly integrated digital signal processor, including a 24-bit stereo ADC with MIC gain amplifiers, a 24-bit stereo ADC with input selector, two 32-bit stereo DACs, 4 stereo & 4 monaural sample rate converters (SRCs) supporting the sampling frequency up to 192kHz, a DIT, two DSPs and a Sub DSP for Audio/HF process. The DSP1 and the DSP2 have 6144step/fs (when fs=48kHz) parallel processing power. The AK7739 is capable of processing sound and voice such as for hands-free function simultaneously because two DSPs are able to work on different but synchronized sampling frequencies. As the AK7739 is a RAM based DSP, it is freely programmable for user requirements, such as acoustic effects and proprietary high performance hands-free function. The AK7739 is available in a space saving 64-pin HTQFP package.

2. Features

☐ Dual DSP (DSP1, DSP2): (Delay RAM areas are shared by DSP1 and DSP2)
- Word Length: 37-bit (Data RAM: Simple floating point)
- Operational Clock 294.912MHz (6144steps, fs= 48kHz)
- Multiplier: 32 x 32 → 64-bit (Double precision arithmetic available)
- Divider: 32 / 32 → 32-bit (Floating point normalization function)
- ALU: 96-bit arithmetic operation (with overflow margin 32-bit)
- Program RAM (PRAM): 10kword x 36-bit (DSP1), 8kword x 36-bit (DSP2)
- Coefficient RAM (CRAM): 6kword x 32-bit (DSP1), 6kword x 32-bit (DSP2)
- Data RAM (DRAM): 6kword x 37-bit (DSP1), 6kword x 37-bit (DSP2)
- Delay RAM (DLRAM): 36kword x 37-bit (DSP1+DSP2 Total)
- JX pins (Interrupt)
- Independent Power Management Function for DSP1 and DSP2

☐ Sub DSP (DSP3):
- Word Length: 37-bit (Data RAM: Simple floating point supported)
- Operational Clock 294.912MHz (6144steps, fs= 48kHz)
- Multiple: 32 x 32 → 64-bit (Double precision arithmetic available)
- Divider: 32 / 32 → 32-bit (Floating point normalization function)
- ALU: 96-bit Arithmetic Operation (with overflow margin 32-bit)
- Program RAM (PRAM): 2kword x 36-bit
- Coefficient RAM (CRAM): 4kword x 32-bit
- Data RAM (DRAM): 6kword x 37-bit

☐ ADC1: 24-bit Stereo ADC with MIC Gain Amplifier
- Sampling Frequency: fs=8kHz to 48kHz
- Channel Independent Analog Gain Amplifiers (-3 to 30dB (3dB step))
- Differential Input, Single-ended Input or Pseudo-differential Input
- ADC Characteristics S/N: 95dB (fs=48kHz, Differential Input, MIC Gain = 0dB)
- Channel Independent Digital Volume (+24 to -103dB, 0.5dB Step, Mute)
- Digital HPF for DC Offset Cancelling
- Low Noise MIC Power Output: 2ch
- 5 types of Digital Filter for Sound Color Selection

☐ ADC2: 24-bit Stereo ADC with Input Selector
- Sampling Frequency: fs=8kHz to 192kHz
- Analog Input Selector: Differential Input, Single-ended Input or Pseudo-differential Input
- ADC Characteristics S/N: 102dB (fs=48kHz, Differential Input)
- Channel Independent Digital Volume (+24 to -103dB, 0.5dB Step, Mute)
- Digital HPF for DC Offset Cancelling
- 5 types of Digital Filter for Sound Color Selection

☐ DAC: Advanced 32-bit DAC
- 2ch x2
- Sampling Frequency: fs=8kHz to 192kHz
- Single-ended Output
- DAC Characteristics S/N: 108dB (fs=48kHz)
- Channel Independent Digital Volume (+12 to -115dB, 0.5dB Step, Mute)
- 4 types of Digital Filter for Sound Color Selection

☐ SRC
- 2ch x 4 (Stereo)
- 1ch x 4 (Monaural) or 2ch x 2 (Stereo)
- FSI = 8kHz ~ 192kHz, FSO= 8kHz ~ 192kHz (FSO/FSI= 0.167 ~ 6.0)

☐ DIT
- S/PDIF, IEC60958, AES/EBU, EIAJ CP1201 Compatible

☐ Digital Interfaces
- Digital Input Port 6 (Max. 96ch @Fs:48kHz TDM / 48ch @Fs:96kHz TDM)
- Digital Output Port 6 (Max. 96ch @Fs:48kHz TDM / 48ch @Fs:96kHz TDM)
- Independent LRCK/BICK Input/output Port x 5
- Data Format: MSB 32, 24-bit/ LSB 24, 20, 16-bit/ I^2S
- Short / Long Frame Supported
- TDM Input / Output Mode (Supported by all ports/ 512 mode x2)
- Digital MIC Input Port (2ch x 1)
- SPI Interface Master Controller

☐ Digital Mixer Circuit (x2)
☐ PLL Circuit
☐ µP Interface: SPI (7MHz Max.) / I^2C (400KHz Fast Mode)
☐ Power Supply:

Digital:	VDD12:	1.14V ~ 1.3V (Typ. 1.2V)
I/F:	TVDD1:	1.7V ~ 3.6V (Typ. 3.3V)
	TVDD2:	1.7V ~ 3.6V (Typ. 3.3V)
	TVDD3:	1.7V ~ 3.6V (Typ. 3.3V)
	AVDD:	3.13V ~ 3.6V (Typ. 3.3V)
	PLLVDD:	3.13V ~ 3.6V (Typ. 3.3V)

☐ Operating Temperature: Ta= -40 ~ 85ºC
☐ Package: 64-pin HTQFP (10mm x 10mm, 0.5mm pitch)

3. Table of Contents

4. Block Diagram

■ Device Block Diagram

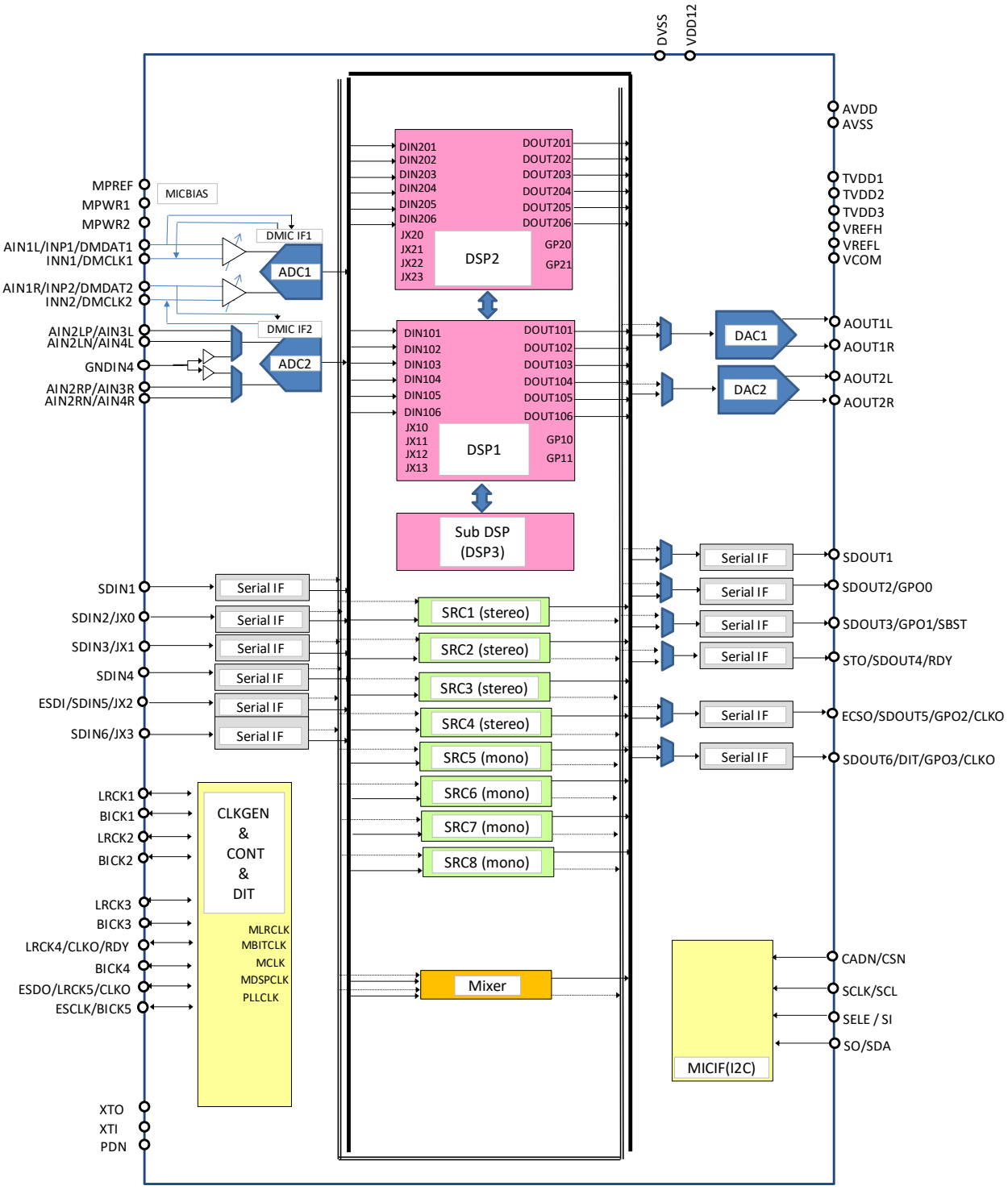
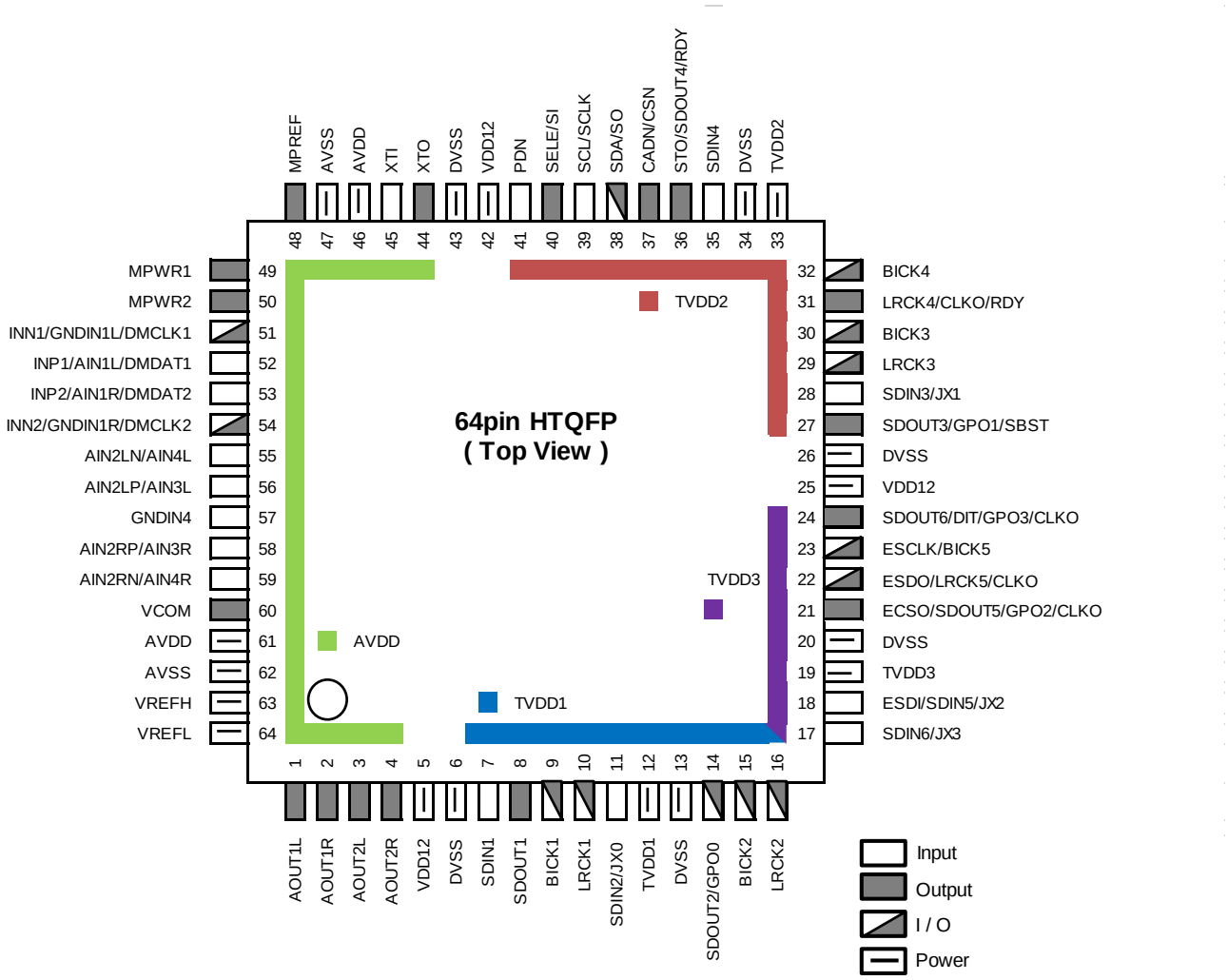


Figure 1. AK7739 Block Diagram

5. Pin Configurations and Functions

■ Pin Layout



■ Pin Functions

No.	Pin Name	I/O	Function	Power Supply
1	AOUT1L	O	DAC1 Lch Output	AVDD
2	AOUT1R	O	DAC1 Rch Output	AVDD
3	AOUT2L	O	DAC2 Lch Output	AVDD
4	AOUT2R	O	DAC2 Rch Output	AVDD
5	VDD12	-	Digital Power Supply Typ. 1.2V (1.14 ~ 1.3V)	-
6	DVSS	-	Digital Ground 0V	-
7	SDIN1	I	Serial Data Input 1	TVDD1
8	SDOUT1	O	Serial Data Output 1	TVDD1
9	BICK1	I/O	Serial Bit Clock 1	TVDD1
10	LRCK1	I/O	LR Channel Selection 1	TVDD1
11	SDIN2	I	Serial Data Input 2	TVDD1
	JX0	I	External Conditional Jump Input (JX0 Input of DSP)	
12	TVDD1	-	Digital IO Power Supply 1 Typ. 3.3V (1.7 ~ 3.6V)	-
13	DVSS	-	Digital Ground 0V	-
14	SDOUT2	O	Serial Data Output 2	TVDD1
	GPO0	O	Programmable Output 0 (GPO0 Output of DSP1)	
15	BICK2	I/O	Serial Bit Clock 2	TVDD1
16	LRCK2	I/O	LR Channel Selection 2	TVDD1
17	SDIN6	I	Serial Data Input 6	TVDD3
	JX3	I	External Conditional Jump Input 3 (JX3 Input of DSP)	
18	ESDI	I	SPI Control Data Input for External Devices (Connect to the SO pin of External Device) (Internally Pulled Down)	TVDD3
	SDIN5	I	Serial Data Input 5	
	JX2	I	External Conditional Jump Input 2 (JX2 input of DSP)	
19	TVDD3	-	Digital IO Power Supply 3 Typ. 3.3V (1.7 ~ 3.6V)	-
20	DVSS	-	Digital Ground 0V	-

No.	Pin Name	I/O	Function	Power Supply
21	ECSO	O	SPI Control Output for External Devices (Connect to the CS pin of External Device)	TVDD3
	SDOUT5	O	Serial Digital Data Output 5	
	GPO2	O	Programmable Output 2 (GPO0 Output of DSP2)	
	CLKO	O	Master Clock Output Pin	
22	ESDO	O	SPI Control Data Output for External Devices (Connect to the SI pin of External Device)	TVDD3
	LRCK5	I/O	LR Channel Selection 5	
	CLKO	O	Master Clock Output	
23	ESCLK	O	SPI Control Clock Output for External Devices (Connect to the SCLK pin of External Device)	TVDD3
	BICK5	I/O	Serial Bit Clock 5	
24	SDOUT6	O	Serial Data Output 6	TVDD3
	DIT	O	DIT Output Pin	
	GPO3	O	Programmable Output 3 (GPO3 Output of DSP2)	
	CLKO	O	Master Clock Output	
25	VDD12	-	Digital Power Supply Typ. 1.2V (1.14 ~ 1.3V)	-
26	DVSS	-	Digital Ground 0V	-
27	SDOUT3	O	Serial Data Output 3	TVDD2
	GPO1	O	Programmable Output 1 (GPO1 Output of DSP1)	
	SBST	O	Self-Boot Status Pin (Valid when the SELE pin = “H”)	
28	SDIN3	I	Serial Data Input 3	TVDD2
	JX1	I	External Conditional Jump Input 1 (JX1 Input of DSP)	
29	LRCK3	I/O	LR Channel Selection 3	TVDD2
30	BICK3	I/O	Serial Bit Clock 3	TVDD2
31	LRCK4	I/O	LR Channel Selection 4	TVDD2
	CLKO	O	Master Clock Output	
	RDY	O	RDY Signal Output	
32	BICK4	I/O	Serial Bit Clock 4	TVDD2
33	TVDD2	-	Digital IO Power Supply 2 Typ. 3.3V (1.7 ~ 3.6V)	-
34	DVSS	-	Digital Ground 0V	-
35	SDIN4	I	Serial Data Input 4	TVDD2

No.	Pin Name	I/O	Function	Power Supply
36	STO	O	Status Signal Output This pin outputs “H” in power down state.	TVDD2
	SDOUT4	O	Serial Data Output 4	
	RDY	O	RDY Signal Output	
37	CADN	I	I²C Mode: I²C I/F Chip Address N Pin This pin must be pulled up or pulled down. Inverted polarity is used as the bus address. I²C Address Selection, connected to DVSS by default. Default Address = 0x38 (CSN pin is logical “low”) Alternative Address = 0x30 (CSN pin is logical “high”) Slave address of A3 (CAD) bit can be set by this pin.	TVDD2
	CSN	I	SPI Mode: Chip Selection N Pin for SPI Interface This pin should be set to “H” in power down state or when not interfacing to a microcomputer.	
38	SDA	I/O	I²C Interface Pin	TVDD2
	SO	O	Serial Data Output for SPI Interface	
39	SCL	I	Serial Data Clock Input for I²C Interface	TVDD2
	SCLK	I	Serial Data Clock Input for SPI Interface	
40	SELE	I	Self-boot Enable Pin (Valid when the CSN pin= “H”)	TVDD2
	SI	I	Serial Data Input for SPI Interface	
41	PDN	I	Power Down N Pin The AK7739 can be powered down by this pin. “L”: Power Down, “H”: Normal Operation This pin should be “L” when power up the AK7739.	TVDD2
42	VDD12	-	Digital Power Supply Typ. 1.2V (1.14 ~ 1.3V)	-
43	DVSS	-	Digital Ground Pin 0V	-
44	XTO	O	Oscillation Circuit Output Connect a crystal oscillator between the XTI pin and the XTO pin. When not using a crystal oscillator, this pin should be open.	AVDD
45	XTI	I	Oscillation Circuit Input Connect a crystal oscillator between the XTI pin and the XTO pin. When not using a crystal oscillator, this pin should be connected to AVSS or connected to external clock.	AVDD
46	AVDD	-	Analog Power Supply Pin Typ. 3.3V (3.13 ~ 3.6V)	-
47	AVSS	-	Analog Ground Pin 0V	-

No.	Pin Name	I/O	Function	Power Supply
48	MPREF	O	Ripple Filter for MIC Power Supply Connect a 1uF ceramic capacitor between this pin and AVSS. Do not connect this pin to external circuits.	AVDD
49	MPWR1	O	Power Supply Output 1 for MIC (“Hi-z” Output in Power-down)	AVDD
50	MPWR2	O	Power Supply Output 2 for MIC (“Hi-z” Output in Power-down)	AVDD
51	INN1	I	ADC1 Lch Differential Inverted Input 1	AVDD
	GNDIN1L	I	ADC1 Lch Pseudo Differential Ground Input 1	
	DMCLK1	O	Digital MIC Clock Output 1	
52	INP1	I	ADC1 Lch Differential Non-inverted Input 1	AVDD
	AIN1L	I	ADC1 Lch Single-ended / Pseudo Differential Input 1	
	DMDAT1	I	Digital MIC Data Input 1	
53	INP2	I	ADC1 Rch Differential Non-inverted Input 2	AVDD
	AIN1R	I	ADC1 Rch Single-ended / Pseudo Differential Input 1	
	DMDAT2	I	Digital MIC Data Input 2	
54	INN2	I	ADC1 Rch Differential Inverted Input 2	AVDD
	GNDIN1R	I	ADC1 Rch Pseudo Differential Ground Input 1	
	DMCLK2	O	Digital MIC Clock Output 2	
55	AIN2LN	I	ADC2 Lch Differential Inverted Input 2	AVDD
	AIN4L	I	ADC2 Lch Single-ended Input 4	
56	AIN2LP	I	ADC2 Lch Differential Non-inverted Input 2	AVDD
	AIN3L	I	ADC2 Lch Single-ended Input 3	
57	GNDIN4	I	ADC2 Pseudo Differential Ground Input 4	AVDD
58	AIN2RP	I	ADC2 Rch Differential Non-inverted Input 2	AVDD
	AIN3R	I	ADC2 Rch Single-ended Input 3	
59	AIN2RN	I	ADC2 Rch Differential Inverted Input 2	AVDD
	AIN4R	I	ADC2 Rch Single-ended Input 4	
60	VCOM	O	Analog Common Voltage Output Connect a 2.2uF ceramic capacitor between this pin and AVSS. Do not connect this pin to external circuits.	AVDD
61	AVDD	-	Analog Power Supply 3.3V (typ)	-
62	AVSS	-	Analog Ground 0V	-
63	VREFH	-	CODEC Analog High Level Reference Pin (Connect to AVDD)	AVDD
64	VREFL	-	CODEC Analog Low Level Reference Pin (Connect to AVSS)	AVDD
-	Exposed Pad	-	The exposed pad on the bottom surface of the package must be connected to the ground.	-

■ Handling of Unused Pins

Table 1. Handling of Unused Pins

Classification	Pin Name	Setting
Analog	AOUT1L, AOUT1R, AOUT2L, AOUT2R, XTO, MPREF, MPWR1, MPWR2, INN1/GNDIN1L/DMCLK1, INP1/AIN1L/DMDAT1, INP2/AIN1R/DMDAT2, INN2/GNDIN1R/DMCLK2, AIN2LN/AIN4L, AIN2LP/AIN3L, GNDIN4, AIN2RP/AIN3R, AIN2RN/AIN4R, VCOM	Open
	XTI	Connect to AVSS
Digital	SDOUT1, SDOUT2/GPO0, ECSO/SDOUT5/GPO2/CLKO, ESDO/LRCK5/CLKO, ESCLK/BICK5, SDOUT6/DIT/GPO3/CLKO, SDOUT3/GPO1/SBST, STO/SDOUT4/RDY, SDA/SO	Open
	SDIN1, BICK1, LRCK1, SDIN2/JX0, BICK2, LRCK2, SDIN6/JX3, ESDI/SDIN5/JX2, SDIN3/JX1, LRCK3, BICK3, LRCK4/CLKO/RDY, BICK4, SDIN4, CADN/CSN, SCL/SCLK, SELE/SI, PDN	Connect to DVSS

Unused I/O pins must be connected appropriately.

■ **Internal Pulled-down Pin Status**

No	Pin Name	Power Down Status PDN pin = "L"	No	Pin Name	Power Down Status PDN pin = "L"
1	AOUT1L	"Hi-Z"	32	BICK4	Input (pulled-down typ.51kΩ)
2	AOUT1R	"Hi-Z"	33	TVDD2	-
3	AOUT2L	"Hi-Z"	34	DVSS	-
4	AOUT2R	"Hi-Z"	35	SDIN4	Input (Hi-Z)
5	VDD12	-	36	STO	"H"
6	DVSS	-		SDOUT4	
7	SDIN1	Input (Hi-Z)		RDY	
8	SDOUT1	"L"	37	CADN	Input (Hi-Z)
9	BICK1	Input (pulled-down typ.51 kΩ)		CSN	
10	LRCK1	Input (pulled-down typ.51 kΩ)	38	SDA	"Hi-Z"
11	SDIN2	Input (Hi-Z)		SO	
	JX0		39	SCL	Input (Hi-Z)
12	TVDD1	-		SCLK	
13	DVSS	-	40	SELE	Input (Hi-Z)
14	SDOUT2	"L"		SI	
	GPO0		41	PDN	Input (forced to "L")
15	BICK2	Input (pulled-down typ.51 kΩ)	42	VDD12	-
16	LRCK2	Input (pulled-down typ.51 kΩ)	43	DVSS	-
17	SDIN6	Input (Hi-Z)	44	XTO	"H"
	JX3		45	XTI	"H" (pulled-up typ.1103kΩ)
18	ESDI	Input (Hi-Z)	46	AVDD	-
			47	AVSS	-
	SDIN5		48	MPREF	"L" (pulled-down typ.111 kΩ)
	JX2		49	MPWR1	"Hi-Z"
19	TVDD3	-	50	MPWR2	"Hi-Z"
20	DVSS	-	51	INN1	"Hi-Z"
21	ECSO	"H"		GNDIN1L	
	SDOUT5			DMCLK1	
	GPO2		52	INP1	"Hi-Z"
	CLKO			AIN1L	
22	ESDO	"L"		DMDAT1	
	LRCK5		53	INP2	"Hi-Z"
	CLKO			AIN1R	
23	ESCLK	"L"		DMDAT2	
	BICK5		54	INN2	"Hi-Z"
24	SDOUT6	"L"		GNDIN1R	
	DIT			DMCLK2	
	GPO3		55	AIN2LN	"Hi-Z"
	CLKO			AIN4L	
25	VDD12	-	56	AIN2LP	"Hi-Z"
26	DVSS	-		AIN3L	
27	SDOUT3	"L"	57	GNDIN4	"Hi-Z"
	GPO1		58	AIN2RP	"Hi-Z"
	SBST			AIN3R	
28	SDIN3	Input (Hi-Z)	59	AIN2RN	"Hi-Z"
	JX1			AIN4R	
29	LRCK3	Input (pulled-down typ.51 kΩ)	60	VCOM	"L" (pulled-down typ.300Ω)
30	BICK3	Input (pulled-down typ.51 kΩ)	61	AVDD	-
31	LRCK4	Input (pulled-down typ.51 kΩ)	62	AVSS	-
	CLKO		63	VREFH	"Hi-Z"
	RDY		64	VREFL	"Hi-Z"

6. Absolute Maximum Ratings

(AVSS = DVSS = 0V; * 1)

Parameter		Symbol	Min.	Max.	Unit
Power Supplies					
Analog		AVDD	-0.3	3.9	V
Digital1(Core)		VDD12	-0.3	1.4	V
Digital2(I/F)		TVDD1	-0.3	3.9	V
Digital3(I/F)		TVDD2	-0.3	3.9	V
Digital4(I/F)		TVDD3	-0.3	3.9	V
Difference (AVSS,DVSS)	(* 1)	ΔGND	-0.3	0.3	
Analog Input Voltage	(* 2)	VINA	-0.3	(AVDD+0.3) or 3.9	V
Digital Input Voltage	(* 3)	VIND1	-0.3	(TVDD1+0.3) or 3.9	V
Digital Input Voltage	(* 4)	VIND2	-0.3	(TVDD2+0.3) or 3.9	V
Digital Input Voltage	(* 5)	VIND3	-0.3	(TVDD3+0.3) or 3.9	V
Operational Temperature		Ta	-40	85	ºC
Storage Temperature		Tstg	-65	150	ºC

Notes:

* 1. All voltages are with respect to ground. AVSS and DVSS must be connected to the same ground.
* 2. The maximum analog input voltage is smaller value between (AVDD+0.3)V and 3.9V.
* 3. The maximum digital input voltage of input or input/output pins for TVDD1 is smaller value between (TVDD1+0.3)V and 3.9V.
* 4. The maximum digital input voltage of input or input/output pins for TVDD2 is smaller value between (TVDD2+0.3)V and 3.9V.
* 5. The maximum digital input voltage of input or input/output pins for TVDD3 is smaller value between (TVDD3+0.3)V and 3.9V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

7. Recommended Operating Condition

(AVSS = DVSS = 0V; * 1)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power Supplies					
Analog	AVDD	3.13	3.3	3.6	V
Digital (1.2V Core)	VDD12	1.14	1.2	1.3	V
Digital (I/F)	TVDD1,2,3	1.7	3.3	3.6	V

Notes:

* 6. VDD12 must be powered up after or at the same time as AVDD and TVDD1-3. VDD12 must be powered down before or at the same time as AVDD and TVDD1-3. The PDN pin should be held “L” when power is supplied. The PDN pin is allowed to be “H” after all power supplies are applied and settled.
* 7. Do not turn off the power supply of the AK7739 with the power supply of the peripheral device turned on. When using the I^2C interface, pull-up resistors of SDA and SCL pins should be connected to TVDD2 or less voltage.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in the datasheet.

8. Electrical Characteristics

■ Analog Characteristics

1. MIC AMP Gain

(Ta=25°C; AVDD=VREFH=TVDD1=TVDD2=TVDD3= 3.3V, VDD12=1.2V; AVSS=VREFL=DVSS=0V)

	Parameter		Min.	Typ.	Max.	Unit
MIC AMP	Input Impedance		17	25	33	kΩ
	Gain	MGNL[3:0]bits=0x0, MGNR[3:0]bits=0x0	-4	-3	-2	dB
		MGNL[3:0]bits=0x1, MGNR[3:0]bits=0x1	-1	0	1	
		MGNL[3:0]bits=0x2, MGNR[3:0]bits=0x2	2	3	4	
		MGNL[3:0]bits=0x3, MGNR[3:0]bits=0x3	5	6	7	
		MGNL[3:0]bits=0x4, MGNR[3:0]bits=0x4	8	9	10	
		MGNL[3:0]bits=0x5, MGNR[3:0]bits=0x5	11	12	13	
		MGNL[3:0]bits=0x6, MGNR[3:0]bits=0x6	14	15	16	
		MGNL[3:0]bits=0x7, MGNR[3:0]bits=0x7	17	18	19	
		MGNL[3:0]bits=0x8, MGNR[3:0]bits=0x8	20	21	22	
		MGNL[3:0]bits=0x9, MGNR[3:0]bits=0x9	23	24	25	
		MGNL[3:0]bits=0xA, MGNR[3:0]bits=0xA	26	27	28	
		MGNL[3:0]bits=0xB, MGNR[3:0]bits=0xB	29	30	31	

2. MIC Bias Output

(Ta=25°C; AVDD =VREFH=TVDD1=TVDD2=TVDD3= 3.3V, VDD12=1.2V; AVSS =VREFL=DVSS=0V)

	Parameter	Min.	Typ.	Max.	Unit
MIC Bias	Output Voltage * 8	2.3	2.5	2.7	V
	Load Resistance	2			kΩ
	Load Capacitance			30	pF
	Output Noise (A-weighted)		-114	-108	dBV

Notes

* 8. The output volume is proportional to AVDD (0.76×AVDD).

3. MIC AMP + ADC1

(Ta=25°C; AVDD=VREFH=TVDD1=TVDD2=TVDD3= 3.3V, VDD12=1.2V; AVSS=VREFL=DVSS=0V; Signal Frequency =1kHz; 24-bit Data; BICK=64fs; Measurement Frequency = 20Hz ~ 20kHz @fs=48kHz); MGNL/R[3:0] bits = 0x1 (0dB)

	Parameter		Min.	Typ.	Max.	Unit
MIC AMP + ADC1	Resolution				24	bit
	Differential Input					
	Full-scale Input Voltage	* 9	±2.55	±2.83	±3.11	Vpp
		* 10	±0.324	±0.357	±0.388	
	S/(N+D) (-1dBFS)	fs=48kHz * 9	75	85		dB
		fs=48kHz * 10		75		
	Dynamic Range (-60dBFS)	fs=48kHz (A-weighted) * 9	87	95		dB
		fs=48kHz (A-weighted)* 10		85		
	S/N	fs=48kHz (A-weighted) * 9	87	95		dB
		fs=48kHz (A-weighted) * 10		85		
	Inter-Channel Isolation * 11		90	105		dB
	Channel Gain Mismatch			0.0	0.3	dB
	PSRR * 13			50		dB
	CMRR * 12		60	75		dB
	Single-ended Input, Pseudo-differential Input					
	Full-scale Input Voltage	* 9	2.55	2.83	3.11	Vpp
		* 10	0.324	0.357	0.388	
	S/(N+D) (-1dBFS)	fs=48kHz * 11	72	82		dB
		fs=48kHz * 10		72		
	Dynamic Range (-60dBFS)	fs=48kHz (A-weighted) * 9	84	92		dB
		fs=48kHz (A-weighted) * 10		82		
	S/N	fs=48kHz (A-weighted) * 9	84	92		dB
		fs=48kHz (A-weighted) * 10		82		
	Inter-Channel Isolation * 11		90	105		dB
	Channel Gain Mismatch			0.0	0.3	dB
	PSRR * 13			50		dB
	CMRR (Pseudo-differential) * 14			70		dB

Notes

* 9. MGNL/R[3:0] bits = 0x1 (0dB). Input full-scale voltage is propotional to AVDD (0.86 x AVDD).
* 10. MGNL/R[3:0] bits = 0x7 (+18dB). Input full-scale voltage is propotional to AVDD (0.108 x AVDD).
* 11. Inter-channel isolation with -1dBFS signal input.
* 12. CMRR is applied to both input signals of differential input with 1kHz, 100mVpp Sine wave.
* 13. PSRR is applied to AVDD and VREFH with 1kHz, 50mVpp Sine wave.
* 14. CMRR is applied 1 kHz 100mVpp sine wave to both pseudo-differential input and pseudo-grand input pins. It is defined as a reference value when applying 100mVpp sine wave to the pseudo-differential input

4. ADC2

(Ta=25°C; AVDD=VREFH=TVDD1=TVDD2=TVDD3= 3.3V, VDD12=1.2V; AVSS =VREFL=DVSS=0V; Signal Frequency=1kHz; 24bit Data; BICK=64fs; Measurement Frequency BW= 20Hz - 20kHz @fs=48kHz; Measurement Frequency BW= 20Hz-40kHz @fs=96kHz,192kHz)

	Parameter		Min.	Typ.	Max.	Unit
ADC2	Resolution				24	bit
	Input Impedance		17	25	33	kΩ
	Differential Input					
	Full-scale Input Voltage * 15		±2.55	±2.83	±3.11	Vpp
	S/(N+D) (-1dBFS)	fs=48kHz	80	90		dB
		fs=96kHz		87		
		fs=192kHz		87		
	Dynamic Range (-60dBFS)	fs=48kHz (A-weighted)	94	102		dB
		fs=96kHz		95		
		fs=192kHz		95		
	S/N	fs=48kHz (A-weighted)	94	102		dB
		fs=96kHz		95		
		fs=192kHz		95		
	Inter-Channel Isolation * 11		90	105		dB
	Channel Gain Mismatch			0.0	0.3	dB
	PSRR * 13			50		dB
	CMRR * 12		60	80		dB
	Single-ended Input, Pseudo-differential Input					
	Full-scale Input Voltage * 16		2.55	2.83	3.11	Vpp
	S/(N+D) (-1dBFS)	fs=48kHz	80	90		dB
		fs=96kHz		87		
		fs=192kHz		87		
	Dynamic Range (-60dBFS)	fs=48kHz (A-weighted)	91	99		dB
		fs=96kHz		92		
		fs=192kHz		92		
	S/N	fs=48kHz (A-weighted)	91	99		dB
		fs=96kHz		92		
		fs=192kHz		92		
	Inter-Channel Isolation * 11		90	105		dB
	Channel Gain Mismatch			0.0	0.3	dB
	PSRR * 13			50		dB
	CMRR (Pseudo-differential) * 14		55	75		dB

Notes

* 15. AIN2LP, AIN2LN, AIN2RP and AIN2RN pins. Input full-scale voltage is proportional to AVDD (0.86 x AVDD).
* 16. AIN3L, AIN3R, AIN4L and AIN4R pins. Input full-scale voltage is proportional to AVDD (0.86 x AVDD).

5. DAC

(Ta=25°C; AVDD=VREFH=TVDD1=TVDD2=TVDD3= 3.3V, VDD12=1.2V; AVSS= VREFL= DVSS= 0V; Signal Frequency = 1kHz; 32-bit Data; BICK=64fs; Measurement Frequency BW=20Hz ~ 20kHz @fs=48kHz; Measurement Frequency BW=20Hz ~ 40kHz @fs=96kHz,192kHz)

	Parameter		Min.	Typ.	Max.	Unit
DAC1 DAC2	Resolution				32	bit
	Output Voltage * 17		2.55	2.83	3.11	Vpp
	S/(N+D) (0dBFS)	fs=48kHz	85	95		dB
		fs=96kHz		92		
		fs=192kHz		92		
	Dynamic Range (-60dBFS)	fs=48kHz (A-weighted)	100	108		dB
		fs=96kHz		101		
		fs=192kHz		101		
	S/N	fs=48kHz (A-weighted)	100	108		dB
		fs=96kHz		101		
		fs=192kHz		101		
	Inter-Channel Isolation (fin=1kHz) * 18		90	110		dB
	Channel Gain Mismatch			0.0	0.7	dB
	Load Resistance * 19		10			kΩ
	Load Capacitance				30	pF
	PSRR * 13			50		dB

Notes

* 17. Full-scale output voltage. The output voltage is proportional to AVDD (AVDD x 0.86).
* 18. Inter-channel isolation between each DAC of Lch and Rch with 0dBFS signal input. (AOUT1L and AOUT1R, AOUT2L and AOUT2R).
* 19. To AC load.

■ SRC1~4

(Ta=25°C; AVDD=TVDD1=TVDD2=TVDD3= 3.3V, VDD12=1.2V; AVSS=DVSS=0V; Signal Frequency= 1kHz; 32-bit Data; Measurement Frequency BW =20Hz ~ FSO/2)

	Parameter	Symbol	Min.	Typ.	Max.	Unit
SRC	Resolution				32	bit
	Input Sample Rate	FSI	8		192	kHz
	Output Sample Rate	FSO	8		192	kHz
	THD+N (Input=1kHz, 0dBFS)					
	Audioモード(SRCFAUDx=1, SRCFECx=0)					
	FSO/FSI=192kHz/48kHz			-132		dB
	FSO/FSI=44.1kHz/48kHz			-131		dB
	FSO/FSI=48kHz/88.2kHz			-131		dB
	FSO/FSI=48kHz/96kHz			-185		dB
	FSO/FSI=44.1kHz/96kHz			-123		dB
	FSO/FSI=48kHz/192kHz			-185		dB
	FSO/FSI=8kHz/48kHz			-185		dB
	Voiceモード(SRCFAUDx=0, SRCFECx=0)					
	FSO/FSI=24kHz/32kHz			-97		dB
	FSO/FSI=16kHz/24kHz			-100		dB
	FSO/FSI=24kHz/44.1kHz			-80		dB
	FSO/FSI=16kHz/44.1kHz			-71		dB
	FSO/FSI=8kHz/32kHz			-177		dB
	Dynamic Range (Input=1kHz, -60dBFS)					
	Audioモード(SRCFAUDx=1, SRCFECx=0)					
	FSO/FSI=192kHz/48kHz			180		dB
	FSO/FSI=44.1kHz/48kHz			184		dB
	FSO/FSI=48kHz/88.2kHz			183		dB
	FSO/FSI=48kHz/96kHz			185		dB
	FSO/FSI=44.1kHz/96kHz			182		dB
	FSO/FSI=48kHz/192kHz			185		dB
	FSO/FSI=8kHz/48kHz			185		dB
	Voiceモード(SRCFAUDx=0, SRCFECx=0)					
	FSO/FSI=24kHz/32kHz			157		dB
	FSO/FSI=16kHz/24kHz			160		dB
	FSO/FSI=24kHz/44.1kHz			140		dB
	FSO/FSI=16kHz/44.1kHz			131		dB
	FSO/FSI=8kHz/32kHz			179		dB
	Dynamic Range (Input=1kHz, -60dBFS, A-weighted) FSO/FSI=44.1kHz/48kHz			186		dB
	Ratio between Input and Output Sample Rate	FSO/FSI	0.167		6	-

■ **SRC5~8**

(Ta=25°C; AVDD=TVDD1=TVDD2=TVDD3= 3.3V, VDD12=1.2V; AVSS=DVSS=0V; Signal Frequency =1kHz; 24-bit Data; Meaasurement Frequency BW= 20Hz ~ FSO/2)

	Parameter	Symbol	Min.	Typ.	Max.	Unit
SRC	Resolution				24	bit
	Input Sample Rate	FSI	8		192	kHz
	Output Sample Rate	FSO	8		192	kHz
	THD+N (Input=1kHz, 0dBFS)					
	Voice Mode (SRCFAUDx=0, SRCFECx=0)					
	FSO/FSI= 16kHz/ 8kHz		-	-125	-	dB
	FSO/FSI= 44.1kHz/ 48kHz		-	-125	-	dB
	FSO/FSI= 24kHz/ 32kHz		-	-95	-	dB
	FSO/FSI= 16kHz/ 24kHz		-	-98	-	dB
	FSO/FSI= 24kHz/44.1kHz		-	-78	-	dB
	FSO/FSI= 16kHz/44.1kHz		-	-69	-	dB
	FSO/FSI= 8kHz/ 32kHz		-	-130	-	dB
	FSO/FSI= 8kHz/ 48kHz		-	-130	-	dB
	Audio Mode (SRCFAUDx=1, SRCFECx=0)					
	FSO/FSI= 24kHz/44.1kHz		-	-120	-	dB
	FSO/FSI= 24kHz/ 48kHz		-	-133	-	dB
	FSO/FSI= 16kHz/44.1kHz		-	-98	-	dB
	Dynamic Range (Input=1kHz, -60dBFS)					
	Voice Mode (SRCFAUDx=0, SRCFECx=0)					
	FSO/FSI= 16kHz/ 8kHz		-	135	-	dB
	FSO/FSI= 44.1kHz/ 48kHz		-	136	-	dB
	FSO/FSI= 24kHz/ 32kHz		-	134	-	dB
	FSO/FSI= 16kHz/ 24kHz		-	117	-	dB
	FSO/FSI= 24kHz/44.1kHz		-	132	-	dB
	FSO/FSI= 16kHz/44.1kHz		-	128	-	dB
	FSO/FSI= 8kHz/ 32kHz		-	130	-	dB
	FSO/FSI= 8kHz/ 48kHz		-	130	-	dB
	Audio Mode (SRCFAUDx=1, SRCFECx=0)					
	FSO/FSI= 24kHz/44.1kHz		-	136	-	dB
	FSO/FSI= 24kHz/ 48kHz		-	135	-	dB
	FSO/FSI= 16kHz/44.1kHz		-	135	-	dB
	Dynamic Range (Input=1kHz, -60dBFS, A-weighted) FSO/FSI=44.1kHz/48kHz		-	137	-	dB
	Ratio between Input and Output Sampling Rate	FSO/FSI	0.167		6	-

■ Power Consumption

(Ta= 25ºC; AVDD=PLLVDD=3.13~3.6V (Typ.=3.3V, Max.=3.6V); VDD12=1.14 ~ 1.3V (Typ.=1.2V, Max.=1.3V); TVDD1=TVDD2=TVDD3=1.7 ~ 3.6V(Typ.=3.3V, Max.=3.6V); (AVSS, DVSS = 0V)

Parameter	Symbol	Min.	Typ.	Max	Unit
Power-Up (* 20) (PDN pin= “H”)	AVDD		30	45	mA
	VDD12		160	500	mA
	TVDD1		5	8	mA
	TVDD2		5	8	mA
	TVDD3		5	8	mA
Power-Down (PDN pin= “L”)	AVDD		0.01		mA
	VDD12		1.5		mA
	TVDD1		0.01		mA
	TVDD2		0.01		mA
	TVDD3		0.01		mA

Note:
* 20. The current of VDD12 changes depending on the system frequency and contents of DSP program.

9. Digital Filter Characteristics

1. ADC1/2 Block

(Ta=-40~85°C; AVDD=3.13~3.6V, TVDD1=TVDD2=TVDD3=1.7~3.6V, VDD12=1.14~1.3V; AVSS =DVSS=0V)

1-1. Sharp Roll-Off Filter (ADxVO bit = "0" (x= 1, 2), ADSD bit = "0", ADSL bit = "0")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband * 21	0dB/-0.06dB	PB	0	-	22.1	kHz
	-3.0dB	PB	-	23.7	-	kHz
Stopband * 21		SB	27.8	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion: 0Hz-20kHz		ΔGD	-	0	-	1/fs
Group Delay * 22		GD	-	20	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	0.9	-	Hz

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband * 21	0dB/-0.06dB	PB	0	-	44.2	kHz
	-3.0dB	PB	-	47.5	-	kHz
Stopband * 21		SB	55.6	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion: 0Hz-40kHz		ΔGD	-	0	-	1/fs
Group Delay * 22		GD	-	20	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	1.9	-	Hz

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband * 21	0dB/-0.04dB	PB	0	-	83.7	kHz
	-3.0dB	PB	-	96.0	-	kHz
Stopband * 21		SB	122.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion: 0Hz-40kHz		ΔGD	-	0	-	1/fs
Group Delay * 22		GD	-	16	-	1/fs
ADC Digital Filter (HPF)						
Frequency Response	-3.0dB	FR	-	3.8	-	Hz

* 21. The passband and stopband frequencies are proportional to fs (sampling rate). High-pass filter (HPF) characteristics are not included.

* 22. Delay time caused by the digital filter calculation. This time is measured from an analog signal input until 24-bit data of both channels are set into the output register. It includes delay time by HPF.

1-2. Slow Roll-Off Filter (ADxVO bit = "0" (x= 1, 2), ADSD bit = "0", ADSL bit = "1")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband * 21	0dB/-0.074dB	PB	0	-	12.5	kHz
	-3.0dB		-	19.2	-	kHz
Stopband * 21		SB	36.5	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion: 0Hz-20kHz		ΔGD	-	0	-	1/fs
Group Delay * 22		GD	-	8	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	0.9	-	Hz

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband * 21	0dB/-0.074dB	PB	0	-	25	kHz
	-3.0dB		-	38.5	-	kHz
Stopband * 21		SB	73	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion: 0Hz-40kHz		ΔGD	-	0	-	1/fs
Group Delay * 22		GD	-	8	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	1.9	-	Hz

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband * 21	0dB/-0.1dB	PB	0	-	31.1	kHz
	-3.0dB		-	62.3	-	kHz
Stopband * 21		SB	145.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion: 0Hz-40kHz		ΔGD	-	0	-	1/fs
Group Delay * 22		GD	-	9	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	3.8	-	Hz

1-3. Short Delay Sharp Roll-Off Filter (ADxVO bit = "0" (x= 1, 2), ADSD bit = "1", ADSL bit = "0")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband * 21	0dB/-0.06dB	PB	0	-	22.1	kHz
	-3.0dB		-	23.7	-	kHz
Stopband * 21		SB	27.8	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion: 0Hz-20kHz		ΔGD	-	-	2.6	1/fs
Group Delay * 22		GD	-	6	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	0.9	-	Hz

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband * 21	0dB/-0.06dB	PB	0	-	44.2	kHz
	-3.0dB		-	47.5	-	kHz
Stopband * 21		SB	55.6	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion: 0Hz-40kHz		ΔGD	-	-	2.6	1/fs
Group Delay * 22		GD	-	6	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	1.9	-	Hz

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband * 21	0dB/-0.04dB	PB	0	-	83.7	kHz
	-3.0dB		-	96.0	-	kHz
Stopband * 21		SB	122.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion: 0Hz-40kHz		ΔGD	-	0	0.2	1/fs
Group Delay * 22		GD	-	7	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	3.8	-	Hz

1-4. Short Delay Slow Roll-Off Filter (ADxVO bit = "0" (x= 1, 2), ADSD bit = "1", ADSL bit = "1")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband * 21	0dB/-0.074dB	PB	0	-	12.5	kHz
	-3.0dB		-	19.2	-	kHz
Stopband * 21		SB	36.5	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion: 0Hz-20kHz		ΔGD	-	-	2.6	1/fs
Group Delay * 22		GD	-	6	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	0.9	-	Hz

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband * 21	0dB/-0.074dB	PB	0	-	25	kHz
	-3.0dB		-	38.5	-	kHz
Stopband * 21		SB	73	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion: 0Hz-40kHz		ΔGD	-	-	2.6	1/fs
Group Delay * 22		GD	-	6	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	1.9	-	Hz

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband * 21	0db/-0.1dB	PB	0	-	31.1	kHz
	-3.0dB		-	63.2	-	kHz
Stopband * 21		SB	145.9	-	-	kHz
Stopband Attenuation		SA	85	-	-	dB
Group Delay Distortion: 0Hz-40kHz		ΔGD	-	-	0.6	1/fs
Group Delay * 22		GD	-	7	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	3.8	-	Hz

1-5. Voice Filter (ADxVO bit = "1" (x= 1, 2))

fs=16kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
VOICE						
Passband * 21	-0.5dB/0.5dB	PB	0	-	6.3	kHz
	-3.0dB		-	6.9	-	kHz
Stopband * 21		SB	8.0	-	-	kHz
Stopband Attenuation		SA	60	-	-	dB
Group Delay Distortion : 0Hz-8kHz		ΔGD	-	0	-	1/fs
Group Delay * 22		GD	-	20	-	1/fs
ADC Digital Filter(HPF)						
Frequency Response	-3.0dB	FR	-	0.3	-	Hz

2. DAC1~2 Block

(Ta=-40-85°C; AVDD= 3.13-3.6V, TVDD1=TVDD2=TVDD3= 1.7-3.6V, VDD12=1.14-1.3V; AVSS=DVSS=0V)

2-1 Sharp Roll-Off Filter (DASD bit = "0", DASL bit = "0")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband * 23	±0.05dB	PB	0		21.7	kHz
	−3.0dB	PB		23.4		kHz
Passband Ripple			-0.0032		0.0032	dB
Stopband * 23			26.3			kHz
Stopband Attenuation * 25 * 26			80			dB
Group Delay * 24			-	27.3	-	1/fs
Digital Filter + SCF + SMF * 25						
Frequency Response: 0 ~ 20.0kHz			-0.3		0.1	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband * 23	±0.05dB	PB	0		43.5	kHz
	−3.0dB	PB		46.8		kHz
Passband Ripple		PR	-0.0032		0.0032	dB
Stopband * 23		SB	52.5	0		kHz
Stopband Attenuation * 25 * 26		SA	80			dB
Group Delay * 24		GD	-	27.3	-	1/fs
Digital Filter + SCF + SMF * 25						
Frequency Response: 0 ~ 40.0kHz			-0.5		0.1	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHARP ROLL-OFF						
Passband * 23	±0.05dB	PB	0		87.0	kHz
	−3.0dB	PB		93.6		kHz
Passband Ripple		PR	-0.0032		0.0032	dB
Stopband * 23		SB	105			kHz
Stopband Attenuation * 25 * 26		SA	80			dB
Group Delay * 22		GD	-	27.3	-	1/fs
Digital Filter + SCF + SMF * 25						
Frequency Response: 0 ~ 80.0kHz			-1.9		0.1	dB

Notes

* 23. The passband and stopband frequencies are proportional to fs (sampling rate).
"PB=0.4535 × fs, SB=0.546 × fs".
* 24. Delay time caused by the digital filter calculation. This time is measured from setting of the 16/24/32-bit impulse data to the input registers to output of the analog peak signal.
* 25. The output level is 0dB with 1kHz, 0dB Sine wave input.
* 26. Band width of Stopband Attenuation ranges from 0kHz to fs.

2-2 Slow Roll-Off Filter (DASD bit = "0", DASL bit = "1")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband * 27	±0.05dB	PB	0		8.8	kHz
	−3.0dB	PB		19.8		kHz
Passband Ripple			-0.043		0.043	dB
Stopband * 23			42.7			kHz
Stopband Attenuation * 25 * 26			73			dB
Group Delay * 24			-	6.8	-	1/fs
Digital Filter + SCF + SMF * 25						
Frequency Response: 0 ~ 20.0kHz			-5.0		0.1	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband * 27	±0.05dB	PB	0		17.7	kHz
	−3.0dB	PB		39.5		kHz
Passband Ripple			-0.043		0.043	dB
Stopband * 23			85.3			kHz
Stopband Attenuation * 25 * 26			73			dB
Group Delay * 24			-	6.8	-	1/fs
Digital Filter + SCF + SMF * 25						
Frequency Response: 0 ~ 40.0kHz			-5.2		0.1	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SLOW ROLL-OFF						
Passband * 27	±0.05dB	PB	0		35.5	kHz
	−3.0dB	PB		79.0		kHz
Passband Ripple			-0.043		0.043	dB
Stopband * 23			171			kHz
Stopband Attenuation * 25 * 26			73			dB
Group Delay * 24			-	6.8	-	1/fs
Digital Filter + SCF + SMF * 25						
Frequency Response: 0 ~ 80.0kHz			-5.9		0.1	dB

Note

* 27. The passband and stopband frequencies are proportional to fs (sampling rate).
"PB=0.185 × fs, SB=0.888 × fs".

2-3 Short Delay Sharp Roll-Off Filter (DASD bit = "1", DASL bit = "0")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband * 23	±0.05dB	PB	0		21.7	kHz
	–3.0dB	PB		23.4		kHz
Passband Ripple			-0.0031		0.0031	dB
Stopband * 23			26.3			kHz
Stopband Attenuation * 25 * 26			80			dB
Group Delay * 24			-	6.3	-	1/fs
Digital Filter + SCF + SMF * 25						
Frequency Response: 0 ~ 20.0kHz			-0.3		0.1	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband * 23	±0.05dB	PB	0		43.5	kHz
	–3.0dB	PB		46.8		kHz
Passband Ripple			-0.0031		0.0031	dB
Stopband * 23			52.5	0		kHz
Stopband Attenuation * 25 * 26			80			dB
Group Delay * 24			-	6.3	-	1/fs
Digital Filter + SCF + SMF * 25						
Frequency Response: 0 ~ 40.0kHz			-0.5		0.1	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SHARP ROLL-OFF						
Passband * 23	±0.05dB	PB	0		87.0	kHz
	–3.0dB	PB		93.6		kHz
Passband Ripple			-0.0031		0.0031	dB
Stopband * 23			105			kHz
Stopband Attenuation * 25 * 26			80			dB
Group Delay * 24			-	6.3	-	1/fs
Digital Filter + SCF + SMF * 25						
Frequency Response: 0 ~ 80.0kHz			-1.9		0.1	dB

2-4 Short Delay Slow Roll-Off Filter (DASD bit = "1", DASL bit = "1")

fs=48kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband * 28	±0.05dB	PB	0		12.0	kHz
	−3.0dB	PB		21.1		kHz
Passband Ripple			-0.05		0.05	dB
Stopband * 23			41.5			kHz
Stopband Attenuation * 25 * 26			82			dB
Group Delay * 24			-	5.3	-	1/fs
Digital Filter + SCF + SMF * 25						
Frequency Response: 0 ~ 20.0kHz			-4.8		0.1	dB

fs=96kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband * 28	±0.05dB	PB	0		24.2	kHz
	−3.0dB	PB		42.1		kHz
Passband Ripple			-0.05		0.05	dB
Stopband * 23			83.0			kHz
Stopband Attenuation * 25 * 26			82			dB
Group Delay * 24			-	5.3	-	1/fs
Digital Filter + SCF + SMF * 25						
Frequency Response: 0 ~ 40.0kHz			-5.0		0.1	dB

fs=192kHz

Parameter		Symbol	Min.	Typ.	Max.	Unit
SHORT DELAY SLOW ROLL-OFF						
Passband * 28	±0.05dB	PB	0		48.4	kHz
	−3.0dB	PB		84.3		kHz
Passband Ripple		PR	-0.05		0.05	dB
Stopband * 23		SB	165.9			kHz
Stopband Attenuation * 25 * 26		SA	82			dB
Group Delay * 24		GD	-	5.3	-	1/fs
Digital Filter + SCF + SMF * 25						
Frequency Response: 0 ~ 80.0kHz			-5.7		0.1	dB

Note

* 28. The passband and stopband frequencies are proportional to fs (sampling rate).
"PB=0.252 × fs, SB=0.864 × fs"

3. SRC1~8 Block

(Ta=-40~85°C; AVDD=3.13~3.6V, TVDD1=TVDD2=TVDD3=1.7~3.6V, VDD12=1.14~1.3V; AVSS =DVSS=0V)

3-1. Audio Mode (SRCFAUDx bit = "1", SRCFECx bit = "0")

Parameter			Symbol	Min.	Typ.	Max.	Unit
Pass-band	-0.01dB	0.980 ≤ FSO/FSI ≤ 6.000	PB	0		0.4583FSI	kHz
	-0.01dB	0.900 ≤ FSO/FSI < 0.990	PB	0		0.4167FSI	kHz
	-0.01dB	0.533 ≤ FSO/FSI < 0.909	PB	0		0.2182FSI	kHz
	-0.01dB	0.490 ≤ FSO/FSI < 0.539	PB	0		0.2177FSI	kHz
	-0.01dB	0.450 ≤ FSO/FSI < 0.495	PB	0		0.1948FSI	kHz
	-0.01dB	0.225 ≤ FSO/FSI < 0.455	PB	0		0.1312FSI	kHz
	-0.50dB	0.167 ≤ FSO/FSI < 0.227	PB	0		0.0658FSI	kHz
Stopband		0.980 ≤ FSO/FSI ≤ 6.000	SB	0.5417FSI			kHz
		0.900 ≤ FSO/FSI < 0.990	SB	0.5021FSI			kHz
		0.533 ≤ FSO/FSI < 0.909	SB	0.2974FSI			kHz
		0.490 ≤ FSO/FSI < 0.539	SB	0.2812FSI			kHz
		0.450 ≤ FSO/FSI < 0.495	SB	0.2604FSI			kHz
		0.225 ≤ FSO/FSI < 0.455	SB	0.1802FSI			kHz
		0.167 ≤ FSO/FSI < 0.227	SB	0.0970FSI			kHz
Passband Ripple		0.225 ≤ FSO/FSI ≤ 6.000	PR			±0.01	dB
		0.167 ≤ FSO/FSI < 0.227	PR			±0.50	dB
Stopband Attenuation		0.225 ≤ FSO/FSI ≤ 6.000	SA	95.2			dB
		0.167 ≤ FSO/FSI < 0.455	SA	85.0			dB
Group Delay (Ts=1/fs) (* 29)			GD		67 (55/FSI+12/FSO)		Ts

* 29. It is the time from a rising edge of input LRCK after data is input to an SRC, to a rising edge of output LRCK just before the data is output when there is no phase difference between input and output LRCK.

3-2. Voice Mode (SRCFAUDx= "0", SRCFECx= "0")

Parameter			Symbol	Min.	Typ.	Max.	Unit
Pass-band	-0.01dB	0.980 ≤ FSO/FSI ≤ 6.000	PB	0		0.4583FSI	kHz
	-0.01dB	0.900 ≤ FSO/FSI < 0.990	PB	0		0.4167FSI	kHz
	-0.50dB	0.711 ≤ FSO/FSI < 0.910	PB	0		0.3420FSI	kHz
	-0.50dB	0.653 ≤ FSO/FSI < 0.718	PB	0		0.3007FSI	kHz
	-0.50dB	0.450 ≤ FSO/FSI < 0.660	PB	0		0.2230FSI	kHz
	-0.50dB	0.327 ≤ FSO/FSI < 0.455	PB	0		0.1417FSI	kHz
	-0.50dB	0.225 ≤ FSO/FSI < 0.330	PB	0		0.1018FSI	kHz
	-0.50dB	0.167 ≤ FSO/FSI < 0.227	PB	0		0.0658FSI	kHz
Stopband		0.980 ≤ FSO/FSI ≤ 6.000	SB	0.5417FSI	0.5417FSI		kHz
		0.900 ≤ FSO/FSI < 0.990	SB	0.5021FSI	0.5021FSI		kHz
		0.711 ≤ FSO/FSI < 0.910	SB	0.3735FSI	0.3735FSI		kHz
		0.653 ≤ FSO/FSI < 0.718	SB	0.3320FSI	0.3320FSI		kHz
		0.450 ≤ FSO/FSI < 0.660	SB	0.2490FSI	0.2490FSI		kHz
		0.327 ≤ FSO/FSI < 0.455	SB	0.1660FSI	0.1660FSI		kHz
		0.225 ≤ FSO/FSI < 0.330	SB	0.1248FSI	0.1248FSI		kHz
		0.167 ≤ FSO/FSI < 0.227	SB	0.0970FSI	0.0970FSI		kHz
Passband Ripple		0.900 ≤ FSO/FSI ≤ 6.000	PR			±0.01	dB
		0.167 ≤ FSO/FSI ≤ 0.910	PR			±0.50	dB
Stopband Attenuation		0.900 ≤ FSO/FSI ≤ 6.000	SA	95.2	95.2		dB
		0.653 ≤ FSO/FSI < 0.909	SA	90.0	90.0		dB
		0.450 ≤ FSO/FSI ≤ 0.660	SA	70.0	70.0		dB
		0.167 ≤ FSO/FSI < 0.455	SA	60.0	60.0		dB
Group Delay (Ts=1/fs) (* 29)			GD		67 (55/FSI+12/FSO)		Ts

3-3. Echo Canceller Mode (SRCFECx= "1")

Parameter			Symbol	Min.	Typ.	Max.	Unit
Passband	-0.01dB	0.167 ≤ FSO/FSI ≤ 6.000	PB	0		0.4583FSI	kHz
Stopband		0.167 ≤ FSO/FSI ≤ 6.000	SB	0.5417FSI			kHz
Passband Ripple		0.167 ≤ FSO/FSI ≤ 6.000	PR			±0.01	dB
Stopband Attenuation		0.167 ≤ FSO/FSI ≤ 6.000	SA	95.2			dB
Group Delay (Ts=1/fs) (* 29)			GD		67 (55/FSI+12/FSO)		Ts

10. DC Characteristics

(Ta=-40~85°C; AVDD=3.13~3.6V, TVDD1=TVDD2=TVDD3=1.7~3.6V, VDD12=1.14~1.3V; AVSS =DVSS=0V)

Parameter		Symbol	Min.	Typ.	Max.	Unit
High-Level Input Voltage 1 (* 30)		VIH1	80%TVDD1			V
Low-Level Input Voltage 1 (* 30)		VIL1			20%TVDD1	V
High-Level Input Voltage 2 (* 31)		VIH2	80%TVDD2			V
Low-Level Input Voltage 2 (* 31)		VIL2			20%TVDD2	V
High-Level Input Voltage 3 (* 32)		VIH3	80%TVDD3			V
Low-Level Input Voltage 3 (* 32)		VIL3			20%TVDD3	V
High-Level Input Voltage A1 (* 33)		VIHA1	80%AVDD			V
Low-Level Input Voltage A1 (* 33)		VILA1			20%AVDD	V
High-Level Input Voltage A2 (* 34)		VIHA2	65%AVDD			V
Low-Level Input Voltage A2 (* 34)		VILA2			35%AVDD	V
SCL, SDA High-Level Input Voltage		VIH4	70%TVDD2			V
SCL, SDA Low-Level Input Voltage		VIL4			30%TVDD2	V
High-Level Output Voltage Iout = -100μA (* 35)		VOH1	TVDD1-0.3			V
Low-Level Output Voltage Iout=100μA (* 35)		VOL1			0.3	V
High-Level Output Voltage Iout= -100μA (* 36)		VOH2	TVDD2-0.3			V
Low-Level Output Voltage Iout=100μA (* 36)		VOL2			0.3	V
High-Level Output Voltage Iout= -100μA (* 37)		VOH3	TVDD3-0.3			V
Low-Level Output Voltage Iout=100μA (* 37)		VOL3			0.3	V
High-Level Output Voltage Iout= -100μA (* 38)		VOHA	AVDD3-0.4			V
Low-Level Output Voltage Iout= 100μA (* 38)		VOLA			0.4	V
SCL, SDA Low-Level Output Voltage	Fast Mode					
	TVDD2 ≥ 2.0V (Iout= 3mA)	VOL4			0.4	V
	TVDD2 < 2.0V (Iout= 3mA)	VOL4			20%TVDD2	V
	Fast Mode Plus					
	TVDD2 ≥ 2.0V (Iout= 20mA)	VOL4			0.4	V
	TVDD2 < 2.0V (Iout= 3mA)	VOL4			20%TVDD2	V
Input Leak Current		Iin			±10	μA

Notes:
* 30. BICK1, LRCK1, BICK2, LRCK2, SDIN1 and SDIN2/JX0 pins
* 31. BICK3, LRCK3, BICK4, LRCK4, SDIN3/JX1, SDIN4, CADN/CSN, SELE/SI, SCLK and PDN pins
* 32. BICK5, LRCK5, SDIN5/JX2 and SDIN6/JX3 pins
* 33. XTI pin
* 34. DMDAT1/2 pins
* 35. SDOUT1, BICK1, LRCK1, BICK2, LRCK2 and SDOUT2/GPO0 pins
* 36. SDOUT3/GPO1/SBST, BICK3, LRCK3, LRCK4/CLKO/RDY, BICK4, STO/SDOUT4/RDY and SO pins
* 37. SDOUT5/GPO2/CLKO, LRCK5/CLKO, BICK5 and SDOUT6/DIT/GPO3/CLKO pins
* 38. DMCLK1/2 pins

11. Switching Characteristics

1. System Clock

(Ta=-40~85°C; AVDD=3.13~3.6V, TVDD1=TVDD2=TVDD3=1.7~3.6V, VDD12=1.14~1.3V; AVSS =DVSS=0V; C_L= 20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
XTI Input Timing					
a) X'tal Oscillator					
Input Frequency	fXTI	11.2896		24.576	MHz
b) XTI Clock Input					
Duty Cycle		40	50	60	%
Input Frequency	fXTI	0.256		24.576	MHz
CLKO Output Timing					
Output Frequency	fCLKO	2.048		24.576	MHz
Duty Cycle	dCLKO		50		%
LRCK/BICK Input Timing (Slave Mode)					
LRCK Input Timing					
Frequency	fs	8		192	kHz
BICK Input Timing					
Frequency (* 39)	fBCLK	0.256		24.576	MHz
Pulse Width Low	tBCLKL	0.4 / fBCLK			ns
Pulse Width High	tBCLKH	0.4 / fBCLK			ns
LRCK/BICK Output Timing (PLL Master Mode)					
LRCK Output Timing					
Frequency	fs	8		192	kHz
Pulse Width High PCM Mode Except PCM Mode	 tLRCKH tLRCKH		 1/fBCLK 50		 ns %
BICK Output Timing					
Frequency (* 39)	fBCLK	0.256		24.576	MHz
Duty	dBCLK		50		%

Note:

* 39. Required to meet the following expression: fBCLK ≥ 2 x fs x (Input/Output Data Length)

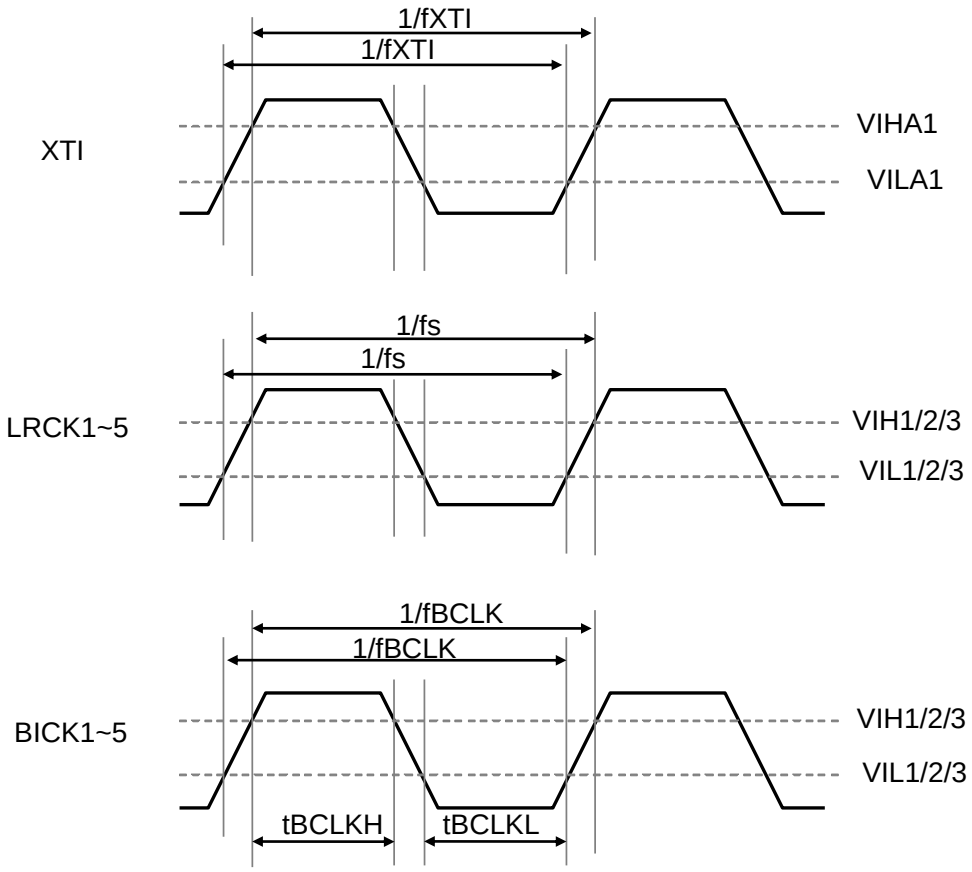


Figure 2. System Clock Timing

2. Power Down

(Ta=-40~85°C; AVDD=3.0~3.6V, TVDD1=TVDD2=TVDD3=1.7~3.6V, VDD12=1.14~1.3V; AVSS =DVSS=0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
PDN Pulse Width (* 40)	tRST	600			ns

Note:

* 40. The PDN pin must be “L” when power up the AK7739.

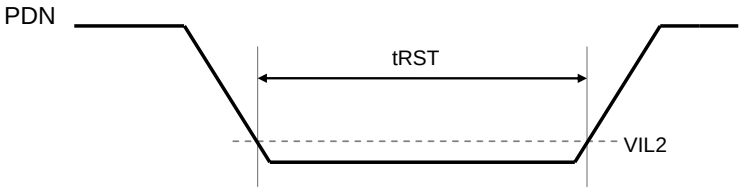


Figure 3. Reset Timing

3. Serial Data Interface (SDIN1 ~ SDIN6, SDOUT1 ~ SDOUT6)

(Ta=-40~85°C; AVDD=3.13~3.6V, TVDD1=TVDD2=TVDD3=1.7~3.6V, VDD12=1.14~1.3V; AVSS =DVSS=0V; C_L=20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Slave Mode					
Delay Time from BICK "↑" to LRCK (* 41)	tBLRD	10			ns
Delay Time from LRCK to BICK "↑" (* 41)	tLRBD	10			ns
Serial Data Input Latch Setup Time	tBSIDS	10			ns
Serial Data Input Latch Hold Time	tBSIDH	5			ns
Delay Time from BICK "↓" to Serial Data Output (* 42, * 43)	tBSOD1			20	ns
Delay Time from BICK "↑"to Serial Data Output (* 41)	tBSOD2	5		30	ns
Master Mode					
BICK frequency	fBCLK		32, 48, 64,128, 256, 512		fs
BICK Duty cycle			50		%
Delay Time from BICK "↓" to LRCK (* 42)	tMBL	-10		10	ns
Serial Data Input Latch Setup Time	tBSIDS	20			ns
Serial Data Input Latch Hold Time	tBSIDH	1			ns
Delay Time from BICK "↓" to Serial Data Output (* 42, * 43)	tBSOD			10	ns

Notes:

* 41. It is measured from BICK "↓" when the BICK polarity is inverted by setting BCKPx bit = "1".
* 42. It is measured from BICK "↑" when the BICK polarity is inverted by setting BCKPx bit = "1".
* 43. Set SDOPHx bit to "1" and the data should be output based on BICK "↑" if BICKx goes faster than 12.288MHz such as when using TDM256 mode with 96kHz sampling frequency in slave mode. SDOPHx bit must be set to "0" in master mode.

1. Slave Mode

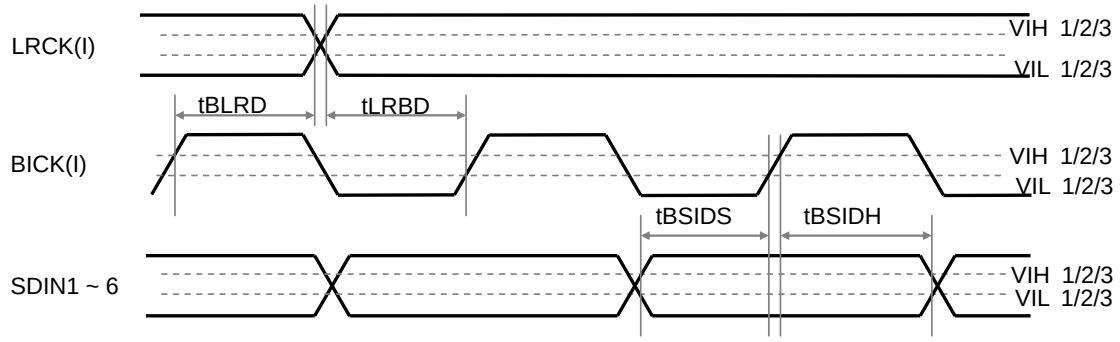


Figure 4. Serial Interface Input Timing in Slave Mode

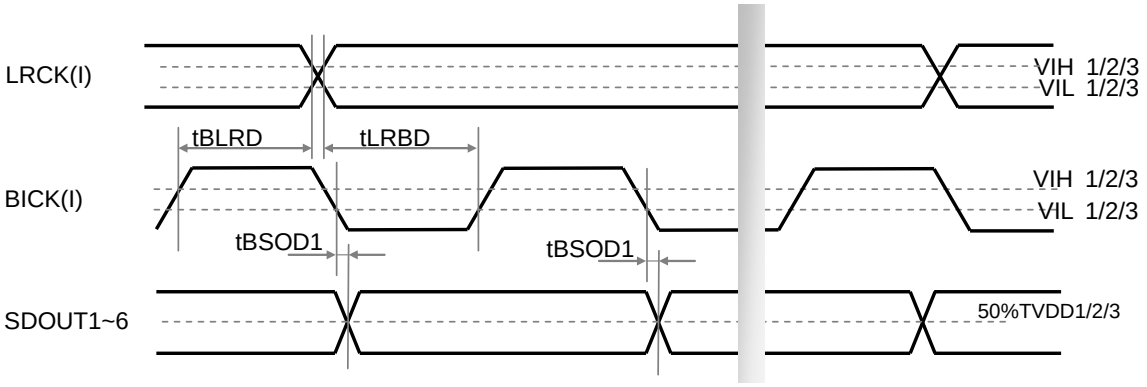


Figure 5. Serial Interface Output Timing in Slave Mode (SDOPHx bit = “0”)

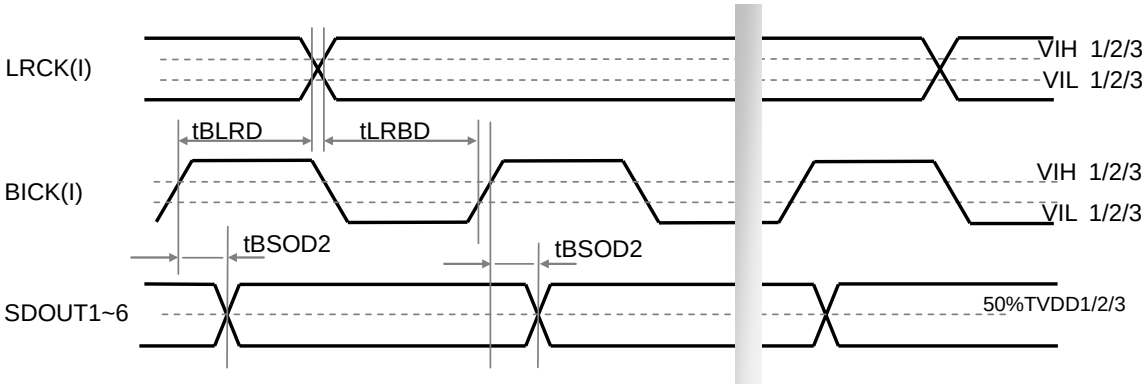


Figure 6. Serial Interface Output Timing in Slave Mode (SDOPHx bit = “1”)

2. Master Mode

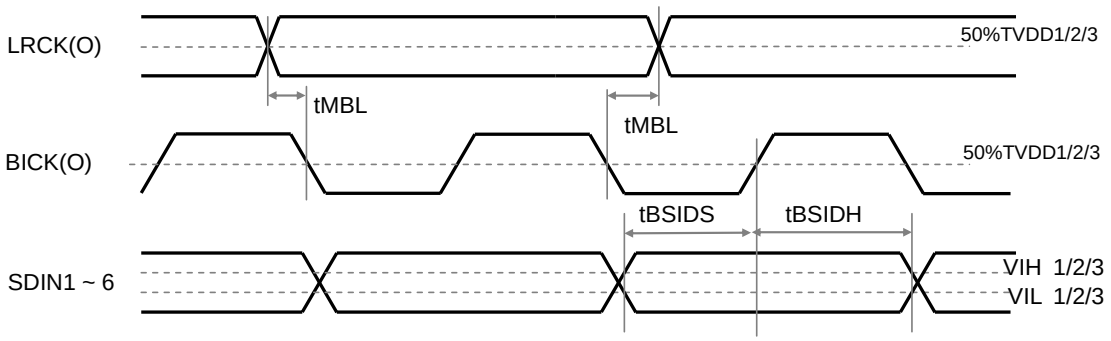


Figure 7. Serial Interface Input Timing in Master Mode

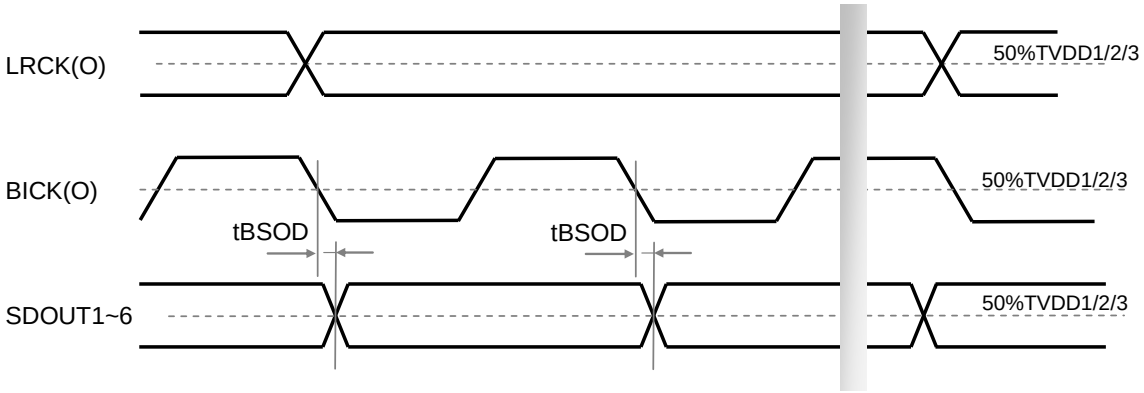


Figure 8. Serial Interface Output Timing in Master Mode (SDOPHx bit = “0”)

4. SPI Interface

(Ta=-40~85°C; AVDD=3.13~3.6V, TVDD1=TVDD2=TVDD3=1.7~3.6V, VDD12=1.14~1.3V; AVSS =DVSS=0V; C_L= 20pF)

1. SPI Low Speed Mode (CKRESETN bit = "0")

Parameter	Symbol	Min.	Typ.	Max.	Unit
µP Interface Signal					
SCLK Frequency (* 45)	fSCLK			3.5	MHz
SCLK Low-level Width	tSCLKL	135			ns
SCLK High- Level Width	tSCLKH	135			ns
Microcontroller → AK7739					
CSN High-Level Width	tWRQH	300			ns
from CSN "↑" to PDN "↑"	tRST	360			ns
from PDN "↑" to CSN "↓"	tIRRQ	1			ms
from CSN "↓ to SCLK "↓"	tWSC	300			ns
from SCLK "↑" to CSN "↑"	tSCW	480			ns
SI Latch Setup Time	tSIS	120			ns
SI Latch Hold Time	tSIH	120			ns
AK7739 → Microcontroller					
Delay Time from SCLK "↓" to SO Output	tSOS			120	ns
SO Output Hold Time from SCLK "↑" (* 44)	tSOH	120			ns

2. SPI Fast Speed Mode (CKRESETN bit = "1" and PL is locked)

Parameter	Symbol	Min.	Typ.	Max.	Unit
µP Interface Timing (SPI mode)					
SCLK Frequency (* 45)	fSCLK			7	MHz
SCLK Low Level Width	tSCLKL	60			ns
SCLK High Level Width	tSCLKH	60			ns
µP → AK7739					
CSN High Level Width	tWRQH	150			ns
From CSN "↑"to PDN "↑"	tRST	180			ns
From PDN "↑"to CSN "↓"	tIRRQ	1			ms
From CSN "↓"to SCLK "↓"	tWSC	150			ns
From SCLK "↑"to CSN "↑"	tSCW	240			ns
SI Latch Setup Time	tSIS	60			ns
SI Latch Hold Time	tSIH	60			ns
AK7739→ µP					
Delay Time from SCLK "↓"to SO Output	tSOS			60	ns
SO Output Hold Time from SCLK "↑" (* 44)	tSOH	60			ns

Note:

* 44. Except when writing the 24th bit of the command code (8-bit command + 16-bit address). Excepts when writing the 8th bit of the read code (8-bit command) in the case of a read command of write preparation data (0x24, 0x26, 0x28).

* 45. Control register access and dummy command generation to switch the interface to SPI from I^2C can always be executed in SPI High Speed mode (Max. 7MHz). Accessing DSP RAM area can be made in SPI Low Speed Mode (Max. 3.5MHz) during clock reset (CKRESETN bit = "0"), and it can be made in SPI High Speed Mode (Max. 7MHz) while PLL is locked (KRESETN bit = "1" and PLL is locked). DLRDY bit must be set to "1" when accessing DSP RAM area while PLL is unlocked. It takes maximum 10ms to lock PLL after setting CKRESETN bit = "0" → "1".

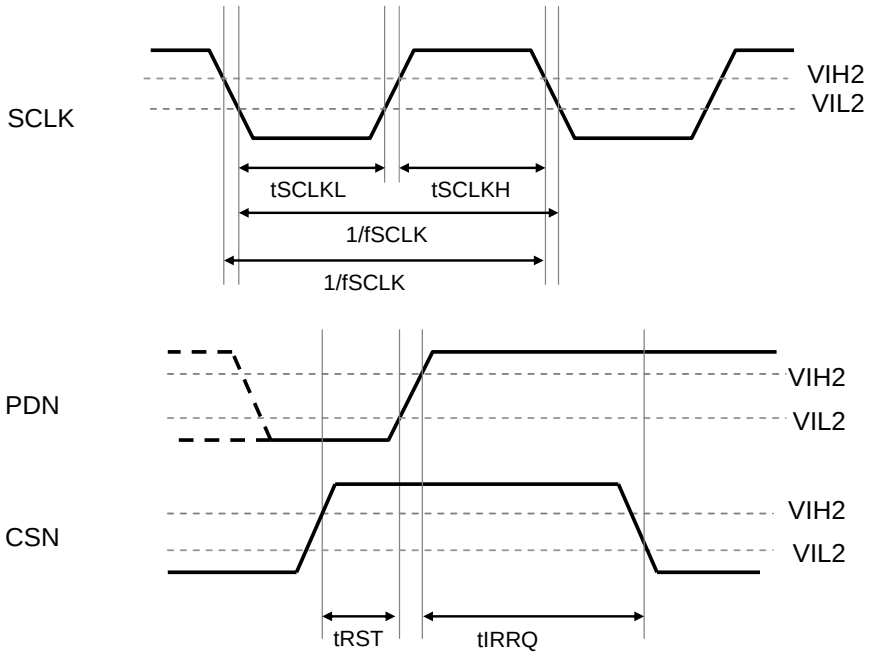


Figure 9. SPI Interface Timing 1

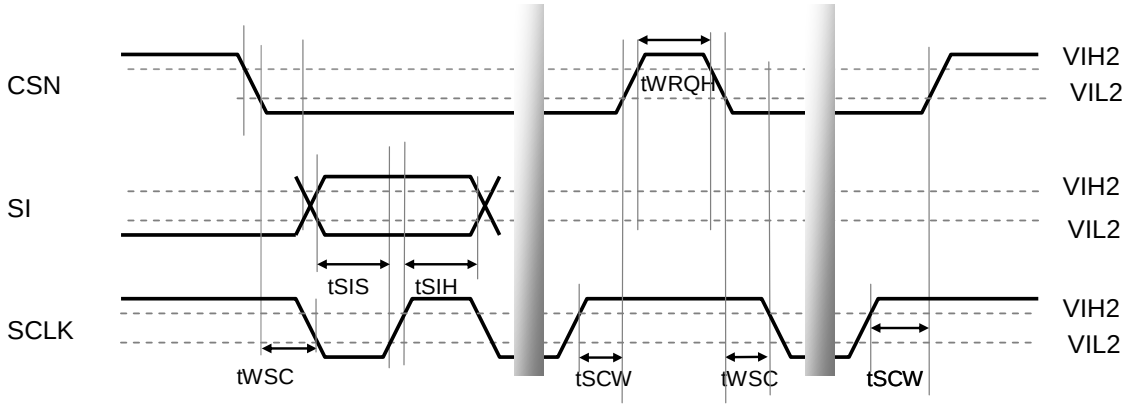


Figure 10. SPI Interface Timing 2 (Microcontroller → AK7739)

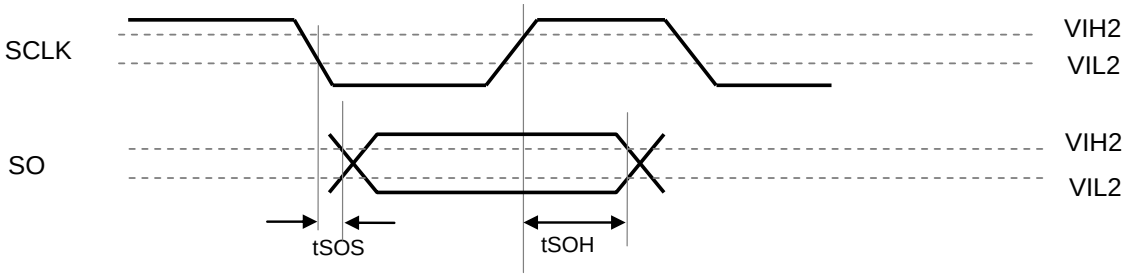


Figure 11. SPI Interface Timing 3 (AK7739 → Microcontroller)

5. I²C Interface

(Ta=-40~85°C; AVDD=3.13~3.6V, TVDD1=TVDD2=TVDD3=1.7~3.6V, VDD12=1.14~1.3V; AVSS =DVSS=0V; C_L= 20pF)

<I²C: Fast Mode>

Parameter	Symbol	Min.	Typ.	Max.	Unit
I²C Timing					
SCL clock frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	µs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.6	-	-	µs
Clock Low Time	tLOW	1.3	-	-	µs
Clock High Time	tHIGH	0.6	-	-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	µs
SDA Hold Time from SCL Falling	tHD:DAT	0	-	-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	µs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	µs
Pulse Width of Spike Noise Suppressed By Input Filter	tSP	0	-	50	ns
SDA Data Valid Time from SCL Falling	tVD:DAT	-	-	0.9	µs
Capacitive load on bus	Cb	-	-	400	pF

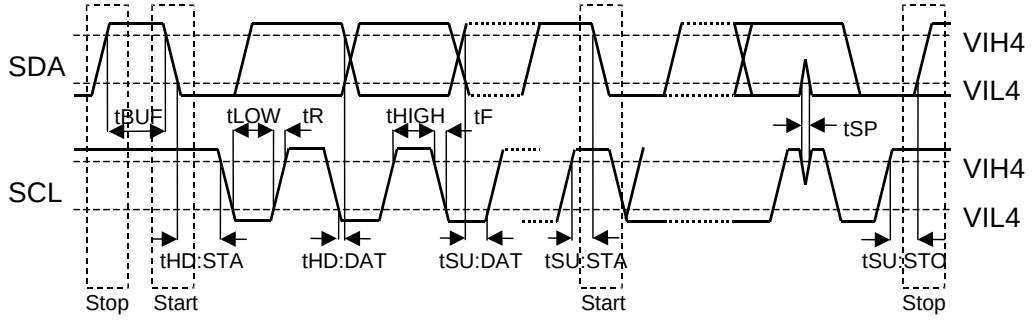


Figure 12. I²C-bus Interface Timing

6. Digital MIC Interface

(Ta=-40~85°C; AVDD=3.13~3.6V, TVDD1=TVDD2=TVDD3= 1.7~3.6V, VDD12=1.14~1.3V; AVSS=DVSS=0V; CL=100pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
DMDAT					
Serial Data Input Latch Setup Time	tDMDS	50			ns
Serial Data Input Latch Hold Time	tDMDH	0			ns
DMCLK					
Clock Frequency (* 46)	fDMCK	0.5	64fs	6.2	MHz
Duty	dDMCK	40	50	60	%
Rising Time	tDMCKR			10	ns
Falling Time	tDMCKF			10	ns

Notes:

* 46. Clock frequency is determined by the sampling rate (fs) selected by FSMODE[4:0] bits.

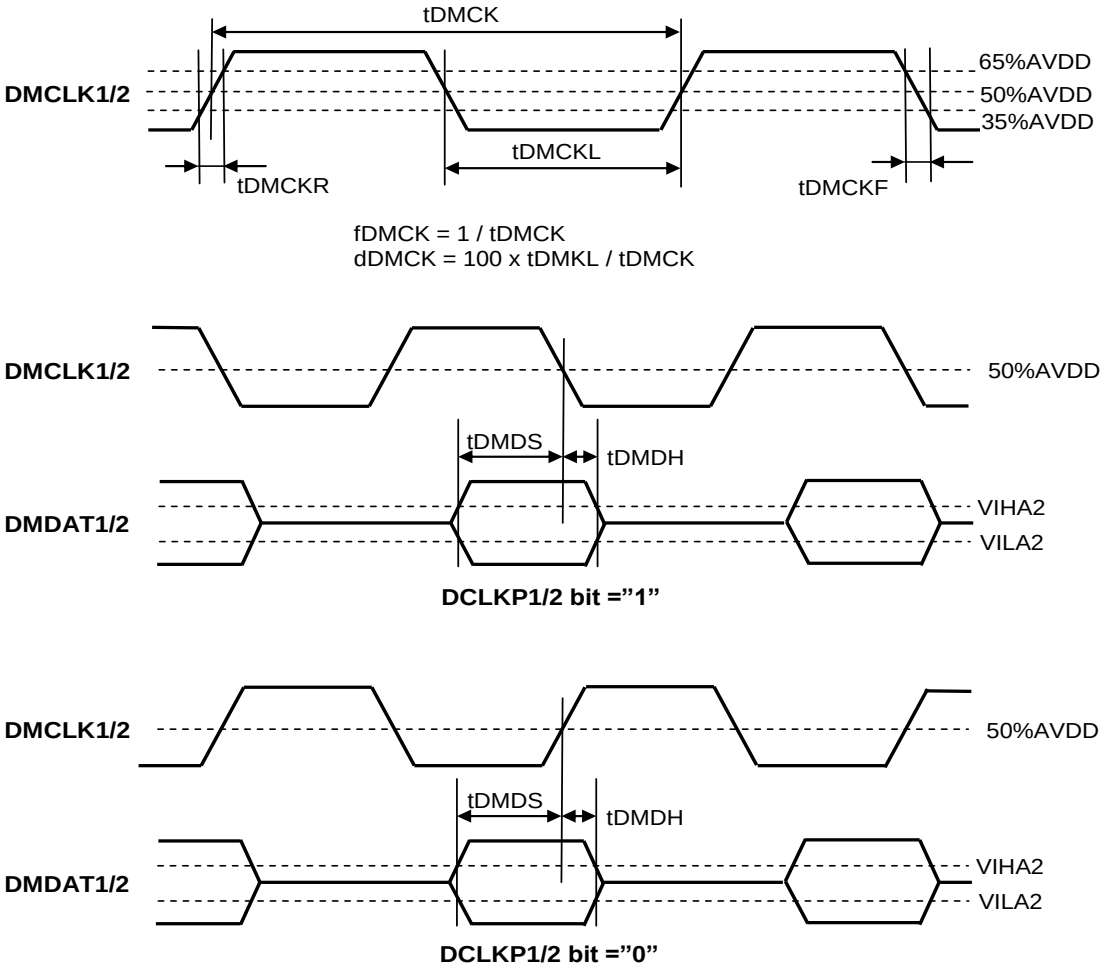


Figure 13. Digital MIC Interface Timing Diagram

7. Master SPI Interface

(Ta = -40~85°C; AVDD = 3.13 ~ 3.6V, TVDD1 = TVDD2 = TVDD3 = 1.7~3.6V, VDD12 = 1.14~1.3V; AVSS = DVSS = 0V; C_L = 20pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Master Mode					
SCLK Frequency	-			6.144	MHz
SCLK Duty (* 47)	-		50		
From ECSO "↓" to ESCLK "↑"	-	80			ns
Delay Time from ESCLK "↓" to ESDO	-	-40		40	ns
ESDI Hold Time from ESCLK "↑"	-	40			ns
ESDI Setup Time from ESCLK "↑"	-	40			ns
Through Mode					
Slave Port → Master Port					
From CSN input to ECSO (Output Delay)	-	0		40	ns
From SCLK input to ESCLK (Output Delay)	-	0		40	ns
From SI input to ESDO (Output Delay)	-	0		40	ns
Master Port → Slave Port					
From ESDI input to SO (Output Delay)	-	0		40	ns

Note:
* 47. Divided by an even number.
It supports a crystal oscillator which is 12.288MHz or less in self boot mode.

13. Recommended External Circuits

■ Connection Diagram

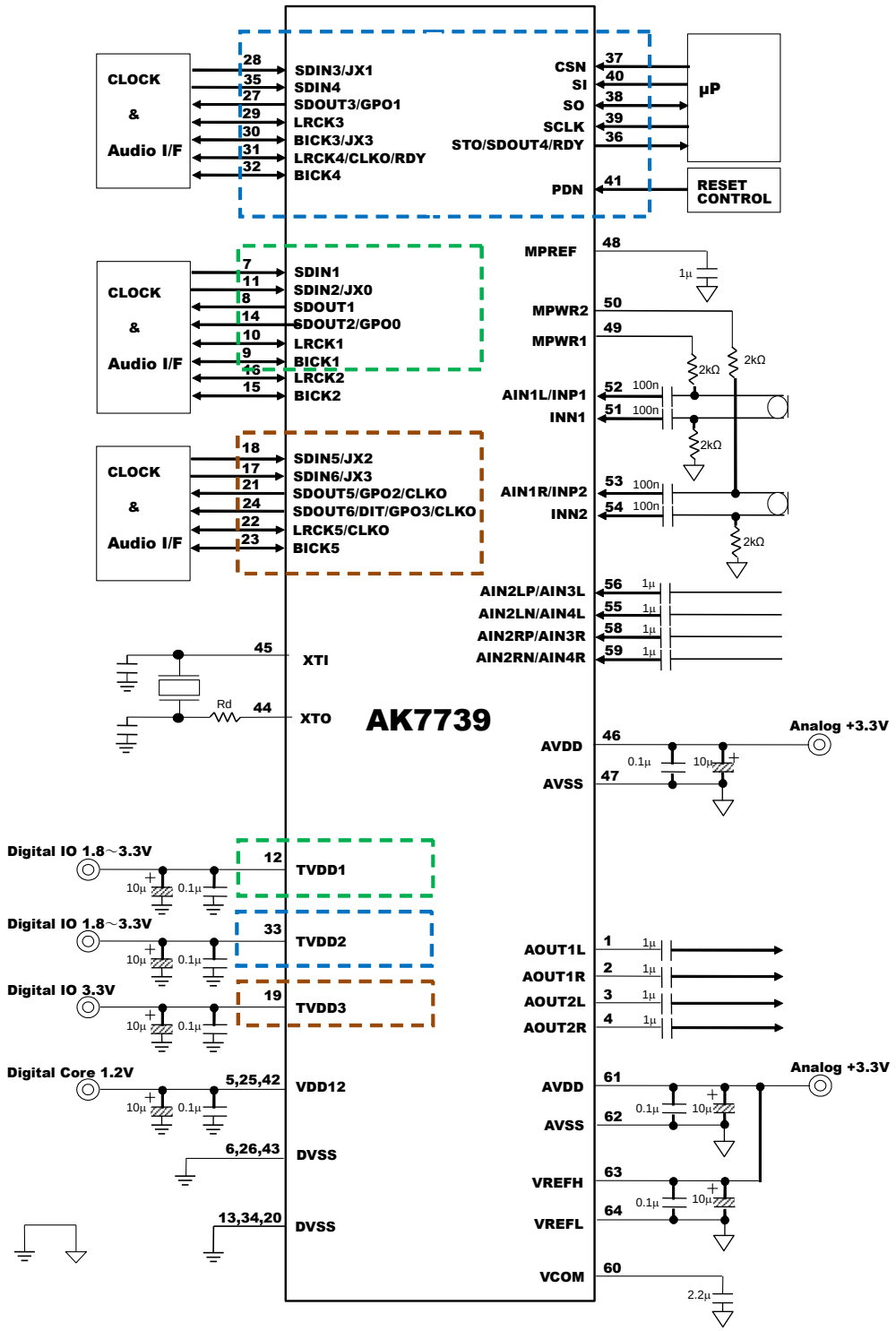


Figure 14. SPI Interface Connection Example

■ Peripheral Circuit

1. Ground

All VSS should be connected to the same ground. Decoupling capacitors, particularly ceramic capacitors of small capacity, should be placed at positions as closed as possible to this device.

2. Reference Voltage

The AVDD voltage controls analog signal range. VCOM is a common voltage of this chip and the VCOM pin outputs AVDD/2. A 2.2µF ceramic capacitor should be connected between the VCOM pin and AVSS.

Do not connect the VCOM pin to any external devices. Digital signal lines, especially clock signal line should be kept away as far as possible from this pin in order to avoid unwanted coupling into the device.

3. Analog Input

The analog input signal is input to the analog modulator of this device. The maximum input voltage at differential input pins is FS = ±(AVDD - AVSS) x 0.86. The maximum input voltage at single-ended input pins is FS = (AVDD - AVSS) x 0.86. When AVDD = 3.3V and AVSS = 0.0V, the input voltage range at differential input pin is ±2.83Vpp and 2.83Vpp at single-ended input pin. The output code format is 2's complements. The internal HPF removes the DC offset.

After power-down is released, the internal operating point level AVDD/2 occurs on analog input pins of this device. Concerning the internal operating point formation circuit, each input pin has impedance of 20kΩ (typ @fs=48kHz). The pins that are connected to AC coupling capacitors require start-up time (time constant).

The analog modulator samples analog inputs at 6.144MHz when fs=48kHz, 96kHz or 192kHz. This device includes an anti-aliasing filter. Therefore, no external low-pass filter is needed in front of the ADC. However, an external low-pass filter should be connected before the ADC for the signal which has large out-of-band noise such as D/A converted signals.

The analog power supply to the device is +3.3V typical. Voltage of AVDD + 0.3V or larger, voltage of AVSS - 0.3V or smaller, and current of 10mA or larger must not be applied to analog input pins. Excessive current will damage the internal protection circuit and will cause latch-up, damaging the IC. Accordingly, if the external analog circuit voltage is ±15V, the analog input pins must be protected from signals which are equal or larger than absolute maximum ratings.

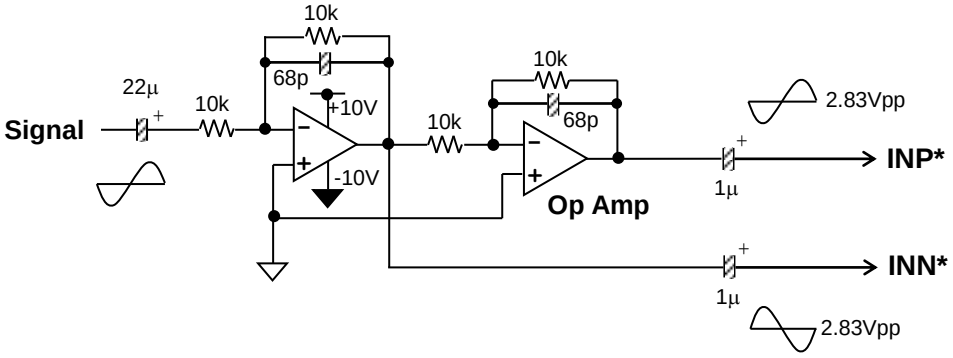


Figure 15. Input Buffer Circuit Example at fs=48kHz (Differential Input)

4. Analog Output

The analog output is single-ended and the output signal range is typically 0.86 x AVDD Vpp centered on VCOM. The digital input data format is two's compliment. Positive full-scale output corresponds to 0x7FFFFFFF (@32bit) input code, Negative full scale is 0x80000000 (@32bit) and VCOM voltage ideally is 0x00000000 (@32bit). The Out-of-Band noise (shaping noise) generated by the internal delta-sigma modulator is attenuated by an integrated switched capacitor filter (SCF) and a continuous time filter (CTF).

5. Connection to Digital Circuit

To minimize the noise from digital circuits, the digital output of the AK7739 must be connected to CMOS or low voltage logic ICs.

6. Cristal Oscillator

The resistor and capacitor values for the oscillator RC circuit are shown blow.

Table 2. Recommended Resistance and Capacitance with Crystal Oscillator

XTAL Oscillator	R1 (Max.)	C0 (Max.)	XTI, XTO pin Capacity
12.288MHz	80Ω	2.5pF	22pF
18.432MHz	80Ω	2.5pF	22pF
24.576MHz	40Ω	2.5pF	15pF

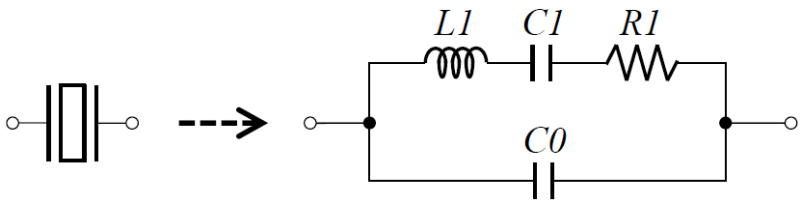
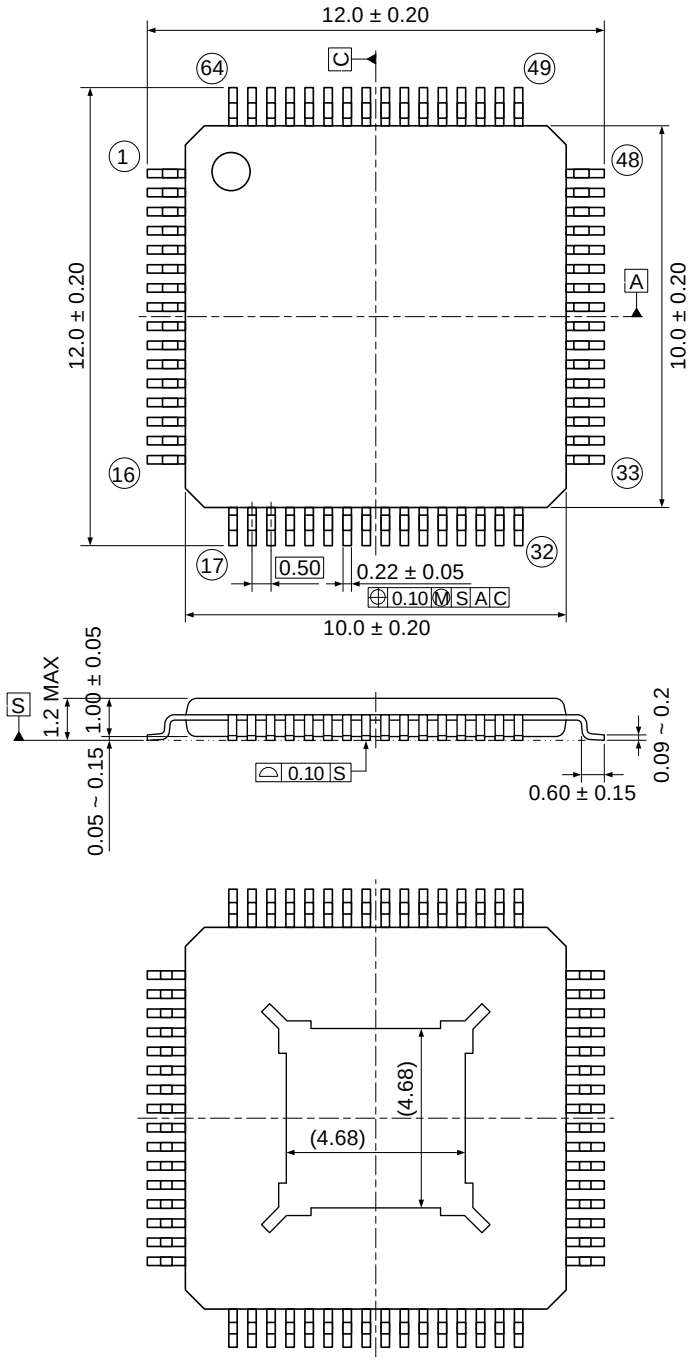


Figure 16. Equivalent Circuit of Cristal Oscillator

14. Package

■ Outline Dimenstions

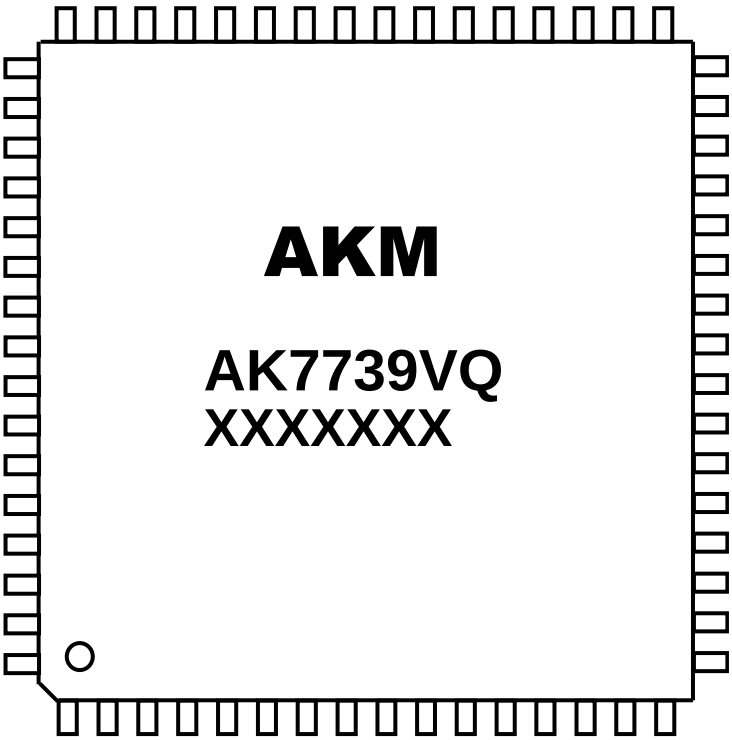
64-pin HTQFP (Unit: mm)



■ Material and Lead Finish

Package molding compound: Epoxy
Lead frame material: Cu
Pin surface treatment: Solder (Pb free) plate

■ **Marking**



1) pin #1 indication
2) Date Code: XXXXXXX(7 digits)
3) Marking Code: AK7739VQ
4) Asahi Kasei Logo

15. Ordering Guide

■ **Ordering Guide**

AK7739VQ	-40 ~ +85ºC	64-pin HTQFP (0.5mm pitch)
AKD7739	AK7739 Evaluation Board	

16. Revision History

Date (Y/M/D)	Revision	Reason	Page	Contents
18/12/06	00	First Edition		
19/06/25	01	Error Correction	13	64pin : Connect to AVDD → Connect to AVSS
19/06/25	01	Error Correction	29	Delete Japanese Character.
19/10/23	02	Error Correction	2	2ch x 4(Stereo) x 2 → 2ch x 4(Stereo) 1ch x 4ch(Monaural) → 1ch x 4(Monaural) 2ch x 4ch(Stereo) → 2ch x 2(Stereo)

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