

## 1. 特性

- 便于使用
  - 外部电阻设置增益(1 到 10,000)
  - 宽供电电压范围( $\pm 2V$  到  $\pm 19V$ )
  - 更高的性能, 相较于 3 运放类仪器放大器
  - 8 PIN MSOP 和 SOIC 封装
  - 低功耗, 1.3mA 静态电流
- 优异的 DC 性能
  - 最大  $\pm 20\mu V$ , 输入失调电压
  - 最大 2.0nA, 输入偏置电流
  - 最低 108dB 共模抑制比( $G = 10$ )
- 低噪声
  - $17nV/\sqrt{Hz}$  @ 1kHz, 输入噪声电压
  - $1.8\mu V_{PP}$  (0.1Hz 到 10Hz)
- 优异的 AC 性能
  - 2038kHz 带宽( $G = 1$ )
- 工作温度
  - $-40^{\circ}C$  到  $125^{\circ}C$

## 2. 应用

- 测量仪器
- ECG 与医疗应用
- 传感器接口
- 数据采集系统
- 工业过程控制
- 电池与移动设备

## 3. 说明

INA103/INA104 是一款低成本, 高精度仪器放大器, 只需要一个外部电阻, 即可设定 1-10000 的增益。INA103/INA104 使用 MSOP-8 和 SOIC-8 封装, 待机功耗低(仅 1.3mA), 非常适宜于电池供电类移动设备。

INA103/INA104 是一款高精度仪器放大器, 仅 0.8ppm 的低非线性度, 最大  $20\mu V$  的输入失调电压, 是高精度数据采集系统的理想选择, 可应用于测量仪器及传感器接口。并且, INA103/INA104 的低噪声、低输入偏置电流、低功耗特性, 使其非常适合应用于医疗应用, 比如 ECG 及血压仪。

低至  $17nV/\sqrt{Hz}$  @ 1kHz,  $1.8\mu V_{PP}$  (0.1Hz 到 10Hz) 的低噪声电压及  $0.45pA/\sqrt{Hz}$  的低噪声电流特性, 使 INA103/INA104 成为预放大的理想选择。

INA103/INA104 非常适合于多路复合应用。有关订购信息, 请参见 Table 1。

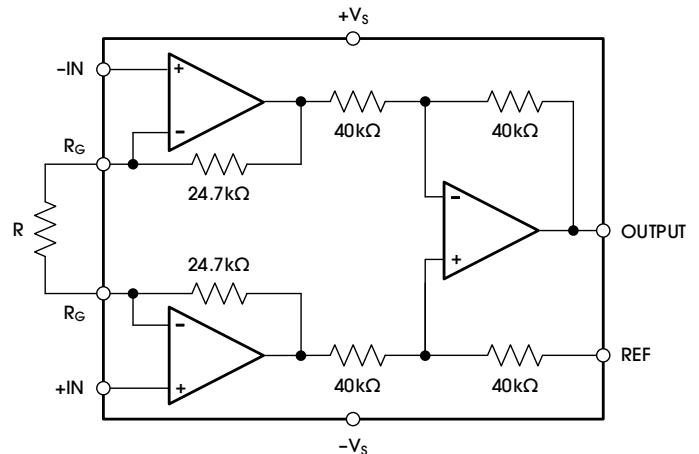


Table 1 lists the order information.

Table 1. Order Information

ORDER NUMBER	CH (#)	PACKAGE	MARK	I <sub>Q</sub> PER CH (TYP) (mA)	BW (kHz)	GAIN	GAIN TYPE	OPERATING TEMP (°C)	PACKAGE OPTION
INA103AMSOP8	1	MSOP-8	INA103	1.3	2038	1-10000	R <sub>E</sub>	-40-125	T/R-4000
INA103ASOIC8 <sup>(1)</sup>	1	SOIC-8	INA103	1.3	2038	1-10000	R <sub>E</sub>	-40-125	T/R-4000
INA104AMSOP8	1	MSOP-8	INA104	1.3	2038	1-10000	R <sub>E</sub>	-40-125	T/R-4000
INA104ASOIC8 <sup>(1)</sup>	1	SOIC-8	INA104	1.3	2038	1-10000	R <sub>E</sub>	-40-125	T/R-4000

Table 2. Family Selection Guide

ORDER NUMBER	CH (#)	PACKAGE	MARK	I <sub>Q</sub> PER CH (TYP) (mA)	BW (kHz)	GAIN	GAIN TYPE	OPERATING TEMP (°C)	PACKAGE OPTION
INA101ASOIC8	1	SOIC-8	INA101	1.56	1300	1-10000	R <sub>E</sub>	-40-85	T/R-4000
INA102ASOIC8	1	SOIC-8	INA102	1.56	1300	1-10000	R <sub>E</sub>	-55-125	T/R-4000
INA111ASOIC8	1	SOIC-8	INA111	0.6	600	1-10000	R <sub>E</sub>	-40-85	T/R-4000
INA112ASOIC8	1	SOIC-8	INA112	0.6	600	1-10000	R <sub>E</sub>	-55-125	T/R-4000
INA201ASOIC8	1	SOIC-8	INA201	1.5	256	10-100	R <sub>E</sub> and OS	-40-85	T/R-4000
INA202ASOIC8	1	SOIC-8	INA202	1.5	256	10-100	R <sub>E</sub> and OS	-55-125	T/R-4000
INA211ASOIC8 <sup>(1)</sup>	1	SOIC-8	INA211	0.6	160	10-100	R <sub>E</sub> and OS	-40-125	T/R-4000
INA212ASOIC8 <sup>(1)</sup>	1	SOIC-8	INA212	0.6	160	10-100	R <sub>E</sub> and OS	-40-125	T/R-4000
INA501LASOIC8 <sup>(1)</sup>	1	SOIC-8	INA501L	1.56	1300	2	Fixed	-40-125	T/R-4000
INA501MASOIC8 <sup>(1)</sup>	1	SOIC-8	INA501M	1.56	1300	5	Fixed	-40-125	T/R-4000
INA501HASOIC8 <sup>(1)</sup>	1	SOIC-8	INA501H	1.56	1300	10	Fixed	-40-125	T/R-4000
INA501NASOIC8 <sup>(1)</sup>	1	SOIC-8	INA501N	1.56	1300	20	Fixed	-40-125	T/R-4000
INA501PASOIC8 <sup>(1)</sup>	1	SOIC-8	INA501P	1.56	1300	25	Fixed	-40-125	T/R-4000
INA501RASOIC8 <sup>(1)</sup>	1	SOIC-8	INA501R	1.56	1300	50	Fixed	-40-125	T/R-4000
INA501SASOIC8 <sup>(1)</sup>	1	SOIC-8	INA501S	1.56	1300	75	Fixed	-40-125	T/R-4000
INA501TASOIC8 <sup>(1)</sup>	1	SOIC-8	INA501T	1.56	1300	100	Fixed	-40-125	T/R-4000
INA501KASOIC8 <sup>(1)</sup>	1	SOIC-8	INA501K	1.56	1300	125	Fixed	-40-125	T/R-4000
INA501JASOIC8 <sup>(1)</sup>	1	SOIC-8	INA501J	1.56	1300	200	Fixed	-40-125	T/R-4000
INA501GASOIC8 <sup>(1)</sup>	1	SOIC-8	INA501G	1.56	1300	250	Fixed	-40-125	T/R-4000
INA501FASOIC8 <sup>(1)</sup>	1	SOIC-8	INA501F	1.56	1300	500	Fixed	-40-125	T/R-4000
INA511LASOIC8 <sup>(1)</sup>	1	SOIC-8	INA511L	0.6	130	2	Fixed	-40-125	T/R-4000
INA511MASOIC8 <sup>(1)</sup>	1	SOIC-8	INA511M	0.6	130	5	Fixed	-40-125	T/R-4000
INA511HASOIC8 <sup>(1)</sup>	1	SOIC-8	INA511H	0.6	130	10	Fixed	-40-125	T/R-4000
INA511NASOIC8 <sup>(1)</sup>	1	SOIC-8	INA511N	0.6	130	20	Fixed	-40-125	T/R-4000
INA511PASOIC8 <sup>(1)</sup>	1	SOIC-8	INA511P	0.6	130	25	Fixed	-40-125	T/R-4000
INA511RASOIC8 <sup>(1)</sup>	1	SOIC-8	INA511R	0.6	130	50	Fixed	-40-125	T/R-4000
INA511SASOIC8 <sup>(1)</sup>	1	SOIC-8	INA511S	0.6	130	75	Fixed	-40-125	T/R-4000
INA511TASOIC8 <sup>(1)</sup>	1	SOIC-8	INA511T	0.6	130	100	Fixed	-40-125	T/R-4000
INA511KASOIC8 <sup>(1)</sup>	1	SOIC-8	INA511K	0.6	130	125	Fixed	-40-125	T/R-4000
INA511JASOIC8 <sup>(1)</sup>	1	SOIC-8	INA511J	0.6	130	200	Fixed	-40-125	T/R-4000
INA511GASOIC8 <sup>(1)</sup>	1	SOIC-8	INA511G	0.6	130	250	Fixed	-40-125	T/R-4000
INA511FASOIC8 <sup>(1)</sup>	1	SOIC-8	INA511F	0.6	130	500	Fixed	-40-125	T/R-4000

Note: Available in the future.

Devices can be ordered via the following two ways:

1. Place orders directly on our website ([www.analogsemi.com](http://www.analogsemi.com)), or;
2. Contact our sales team by mailing to [sales@analogsemi.com](mailto:sales@analogsemi.com).

## 4. PIN CONFIGURATION AND FUNCTIONS

Figure 1 illustrates the pin configuration.

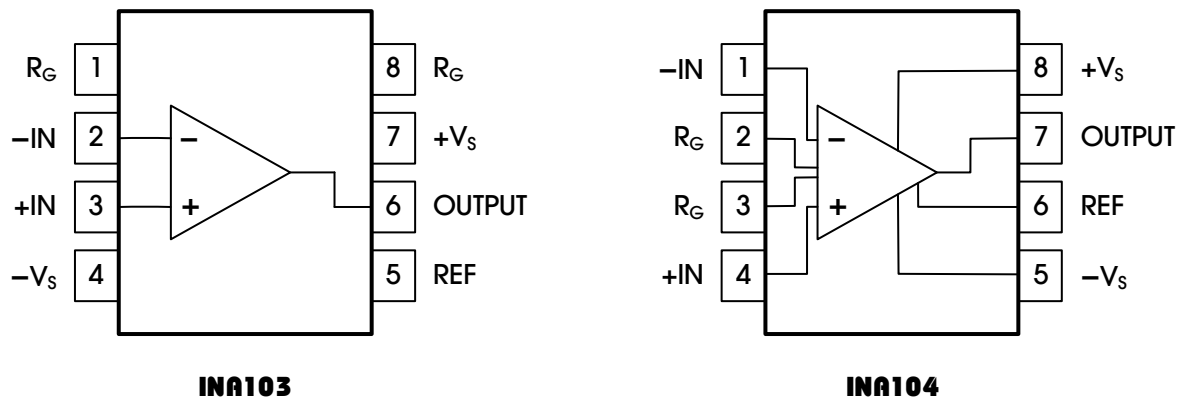


Figure 1. Pin Configuration

Table 3 lists the pin functions.

Table 3. Pin Functions

POSITION		NAME	TYPE	DESCRIPTION
INA103	INA104			
1, 8	2, 3	$R_G$	Analog output	Connect a resistor between two $R_G$ to set gain. See more information in the <a href="#">GAIN SELECTION</a> section.
2	1	$-IN$	Analog input	Signal negative input
3	4	$+IN$	Analog input	Signal positive input
4	5	$-V_S$	Power supply	Negative power supply
5	6	REF	Analog input	Output reference voltage input
6	7	OUTPUT	Analog output	Output
7	8	$+V_S$	Power supply	Positive power supply

## 5. SPECIFICATIONS

### 5.1 ABSOLUTE MAXIMUM RATINGS

Table 4 lists the absolute maximum ratings of the INA103/INA104.

Table 4. Absolute Maximum Ratings

PARAMETER	DESCRIPTION	MIN	MAX	UNITS
Voltage	Supply		±20	V
	Input voltage	$-V_S - 0.3$	$+V_S + 0.3$	V
Current	Any pin except power supply	-10	+10	mA
Output Short-Circuit Duration		Indefinite		
Temperature	Operating, $T_A$	-40	125	°C
	Storage, $T_{stg}$ , $Q$	-65	150	
	Soldering, 10s		300	

Note: Stresses beyond those listed under Table 4 may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Table 6. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 5.2 ESD RATINGS

Table 5 lists the ESD ratings of the INA103/INA104.

Table 5. ESD Ratings

PARAMETER	SYMBOL	DESCRIPTION	VALUE	UNITS
Electrostatic Discharge	$V_{(ESD)}$	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±1500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000	

Note 1: The JEDEC document JEP155 indicates that 500V HBM allows safe manufacturing with a standard ESD control process.

Note 2: The JEDEC document JEP157 indicates that 250V CDM allows safe manufacturing with a standard ESD control process.

### 5.3 RECOMMENDED OPERATING CONDITIONS

Table 6 lists the recommended operating conditions for the INA103/INA104.

Table 6. Recommended Operating Conditions

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNITS
Operating Voltage Range	Split supply	±2.25	±18	±19	V
	Single supply	4.5	36	38	V
Specified Temperature Range		-40		125	°C

### 5.4 THERMAL INFORMATION

Table 7 lists the thermal information for the INA103/INA104.

Table 7. Thermal Information

PARAMETER	SYMBOL	MSOP-8	SOIC-8	UNITS
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	145	90.6	°C/W
Junction-to-Board Thermal Resistance	$R_{\theta JB}$	83.3	47.6	°C/W
Junction-to-Top Characterization Parameter	$\Psi_{JT}$	1.7	3.6	°C/W
Junction-to-Board Characterization Parameter	$\Psi_{JB}$	81.7	47	°C/W
Junction-to-Case (Top) Thermal Resistance	$R_{\theta JC(top)}$	48.3	35	°C/W

### 5.5 ELECTRICAL CHARACTERISTICS

Table 8 lists the electrical characteristics of INA103/INA104. Typical at 25°C,  $V_S = \pm 18V$ , and  $R_L = 2k\Omega$  to GND, unless otherwise noted.

Table 8. Electrical Characteristics

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>GAIN</b>						
Gain Range		$G = 1 + (49.4k\Omega / R_G)$	1		10K	
Gain Error <sup>(1)</sup>		$V_{OUT} = \pm 10V, G = 1$		0.2	0.2	%
		$V_{OUT} = \pm 10V, G = 10$		0.3	0.4	%
		$V_{OUT} = \pm 10V, G = 100$		0.3	0.7	%
		$V_{OUT} = \pm 10V, G = 1000$		0.3	0.5	%
Nonlinearity		$V_{OUT} = -10V$ to $+10V, G = 1, R_L = 10k\Omega$		0.8		ppm
		$V_{OUT} = -10V$ to $+10V, G = 10, R_L = 10k\Omega$		8		ppm
		$V_{OUT} = -10V$ to $+10V, G = 100, R_L = 10k\Omega$		15		ppm
		$V_{OUT} = -10V$ to $+10V, G = 1000, R_L = 10k\Omega$		30		ppm
Gain vs. Temperature		$G = 1^{(5)}$		0.15	0.4	ppm/°C
		Gain > 1 <sup>(1)(5)</sup>		9	32	ppm/°C
<b>VOLTAGE OFFSET<sup>(2)</sup></b>						
Input Offset, $V_{OSI}$		$V_S = \pm 18V$		±4	±20	μV
		$V_S = \pm 2V$ to $\pm 19V$ , overtemperature <sup>(5)</sup>			±45	μV
		$V_S = \pm 2V$ to $\pm 19V$ , average TC <sup>(5)</sup>		±0.1		μV/°C
Output Offset, $V_{OSO}$		$V_S = \pm 18V$		±130	±300	μV
		$V_S = \pm 2V$ to $\pm 19V$ , overtemperature <sup>(5)</sup>			±450	μV
		$V_S = \pm 2V$ to $\pm 19V$ , average TC <sup>(5)</sup>		±0.4		μV/°C
Offset Referred to The Input vs. Supply (PSR)		$V_S = \pm 2V$ to $\pm 20V, G = 1$	104	111		dB
		$V_S = \pm 2V$ to $\pm 20V, G = 1$ , overtemperature <sup>(5)</sup>	100			dB
		$V_S = \pm 2V$ to $\pm 20V, G = 10$	123	131		dB
		$V_S = \pm 2V$ to $\pm 20V, G = 10$ , overtemperature <sup>(5)</sup>	120			dB
		$V_S = \pm 2V$ to $\pm 20V, G = 100$	130	147		dB
		$V_S = \pm 2V$ to $\pm 20V, G = 100$ , overtemperature <sup>(5)</sup>	130			dB
		$V_S = \pm 2V$ to $\pm 20V, G = 1000$	130	156		dB
		$V_S = \pm 2V$ to $\pm 20V, G = 1000$ , overtemperature <sup>(5)</sup>	130			dB
<b>INPUT CURRENT</b>						
Input Bias Current				0.6	2	nA
		Overtemperature <sup>(5)</sup>			10	nA
Input Offset Current				0.1	1	nA
		Overtemperature <sup>(5)</sup>			4.0	nA
<b>INPUT</b>						
Input Impedance		Differential		34    5		$G\Omega\_pF$
		Common-Mode		34    6		$G\Omega\_pF$
Input Voltage Range <sup>(3)</sup>		$V_S = \pm 2V$ to $\pm 19V$	$-V_S + 0.1$		$+V_S - 2$	V

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
<b>COMMON-MODE REJECTION</b>						
Common-Mode Rejection Ratio DC		$V_{CM} = (-V_S + 0.1V) \text{ to } (+V_S - 2V)$ , $G = 1$	88	148		dB
		$V_{CM} = (-V_S + 0.1V) \text{ to } (+V_S - 2V)$ , $G = 1$ , overtemp <sup>(5)</sup>	83			dB
		$V_{CM} = (-V_S + 0.1V) \text{ to } (+V_S - 2V)$ , $G = 10$	108	161		dB
		$V_{CM} = (-V_S + 0.1V) \text{ to } (+V_S - 2V)$ , $G = 10$ , overtemp <sup>(5)</sup>	103			dB
		$V_{CM} = (-V_S + 0.1V) \text{ to } (+V_S - 2V)$ , $G = 100$	129	163		dB
		$V_{CM} = (-V_S + 0.1V) \text{ to } (+V_S - 2V)$ , $G = 100$ , overtemp <sup>(5)</sup>	123			dB
		$V_{CM} = (-V_S + 0.1V) \text{ to } (+V_S - 2V)$ , $G = 1000$	136	163		dB
		$V_{CM} = (-V_S + 0.1V) \text{ to } (+V_S - 2V)$ , $G = 1000$ , overtemp <sup>(5)</sup>	132			dB
<b>OUTPUT</b>						
Output Swing		$R_L = 10k\Omega$ , $V_S = \pm 2V \text{ to } \pm 19V$ , overtemperature <sup>(5)</sup>	$-V_S + 0.2$		$+V_S - 0.3$	V
Short Circuit Current		Overtemperature		$\pm 19$		mA
<b>DYNAMIC RESPONSE</b>						
Small Signal -3dB Bandwidth		$G = 1$		2038		kHz
		$G = 10$		417		kHz
		$G = 100$		53		kHz
		$G = 1000$		4		kHz
Slew Rate		$G = 1$ , 10V step		2		V/ $\mu$ s
		$G = 100$ , 10V step		1		V/ $\mu$ s
<b>NOISE</b>						
Voltage Noise, 1kHz <sup>(4)</sup>		Input, Voltage Noise, $e_{ni}$		17		nV/ $\sqrt{\text{Hz}}$
		Output, Voltage Noise, $e_{no}$		63		nV/ $\sqrt{\text{Hz}}$
RTI, 0.1Hz to 10Hz		$G = 1$		1.8		$\mu$ V <sub>PP</sub>
		$G = 100$		0.4		$\mu$ V <sub>PP</sub>
Current Noise		$f = 1\text{kHz}$		450		fA/ $\sqrt{\text{Hz}}$
<b>REFERENCE INPUT</b>						
$R_{IN}$				80		k $\Omega$
Voltage Range			$-V_S$		$+V_S$	V
Reference Gain to Output				10	41	$\mu$ V/V
<b>POWER SUPPLY</b>						
Operating Range			$\pm 2$		$\pm 19$	V
Quiescent Current		$V_S = \pm 2V \text{ to } \pm 19V$		1.3	1.5	mA
Overtemperature					1.6	mA
<b>TEMPERATURE RANGE</b>						
For Specified Performance			$-40$		$+125$	$^{\circ}\text{C}$

Note 1: Does not include effects of external resistor  $R_G$ .

Note 2: Total RTI Error =  $V_{OSI} + V_{OSO} / G$

Note 3: One input grounded.  $G = 1$ .

Note 4: Total RTI Noise =  $\sqrt{e_{ni}^2 + (e_{no} / G)^2}$

Note 5: All devices are 100% production tested at  $T_A = +25^{\circ}\text{C}$ . All temperature limits are guaranteed by bench test lot.

## 6. TYPICAL CHARACTERISTICS

$T_A = 25^\circ\text{C}$ ,  $V_S = \pm 18\text{V}$ ,  $R_L = 2\text{k}\Omega$ , unless otherwise noted.

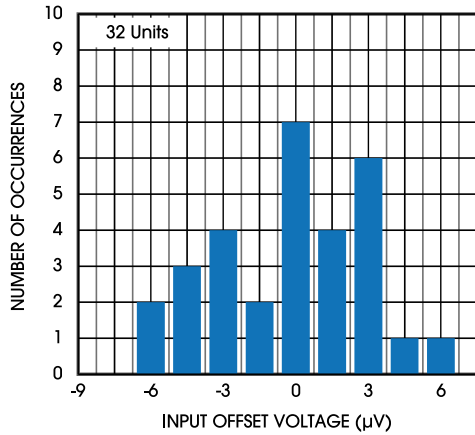


Figure 2. Typical Distribution of Input Offset Voltage

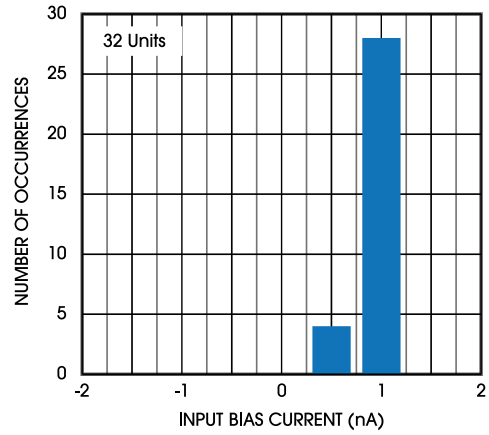


Figure 3. Typical Distribution of Input Bias Current

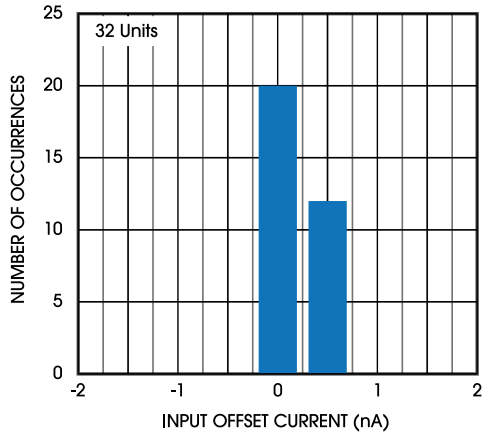


Figure 4. Typical Distribution of Input Offset Current

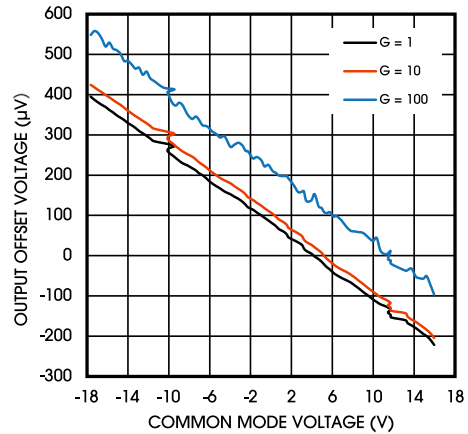


Figure 5. Input Offset Voltage vs. Common Mode Voltage

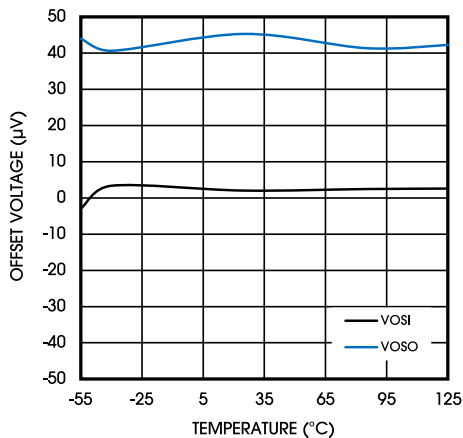


Figure 6. Input Offset Voltage vs. Temperature

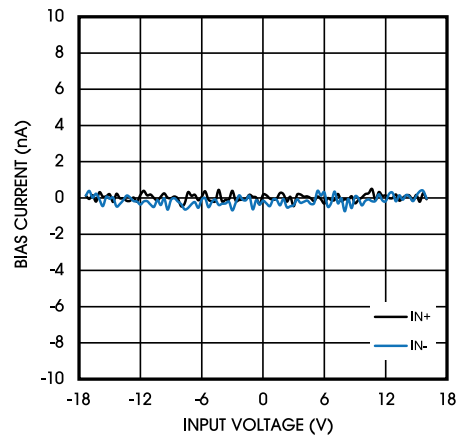


Figure 7. Input Bias Current vs. Common Mode Voltage ( $25^\circ\text{C}$ )

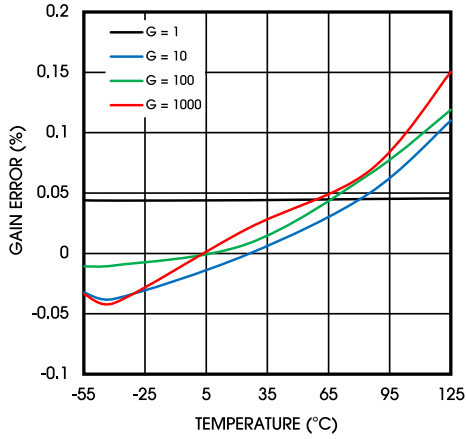


Figure 8. Gain vs. Temperature

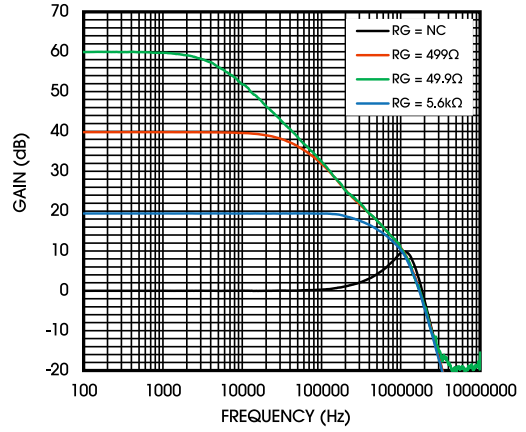


Figure 9. Gain vs. Frequency

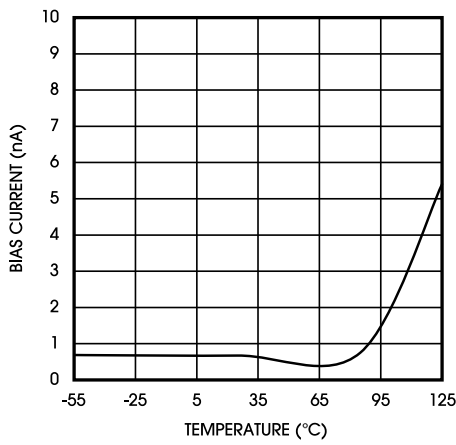


Figure 10. Bias Current vs. Temperature

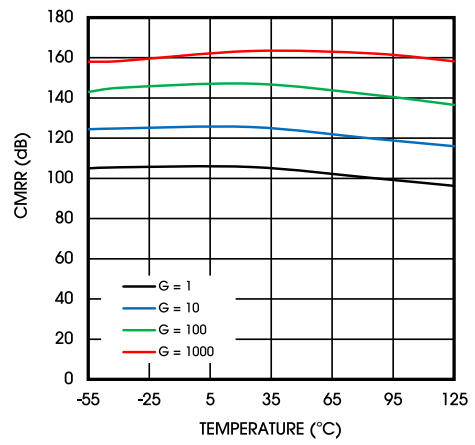


Figure 11. CMRR vs. Temperature

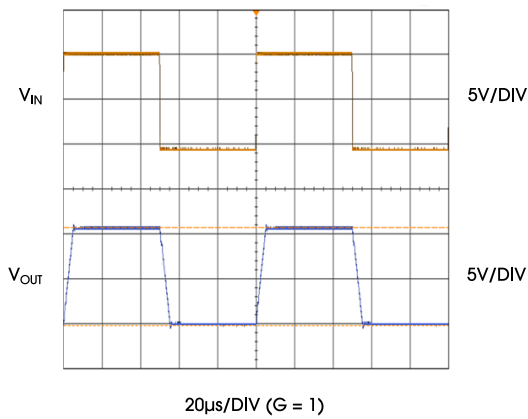


Figure 12. Large Signal Response (G = 1)

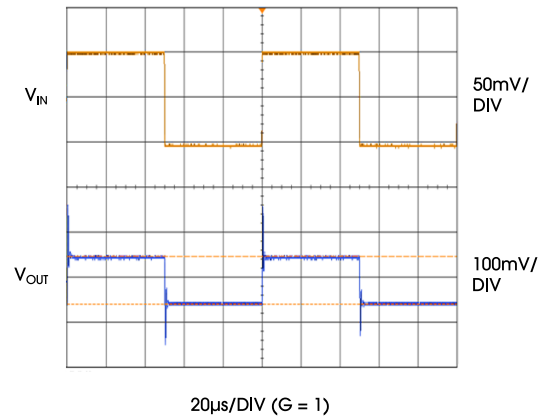


Figure 13. Small Signal Response (G = 1)

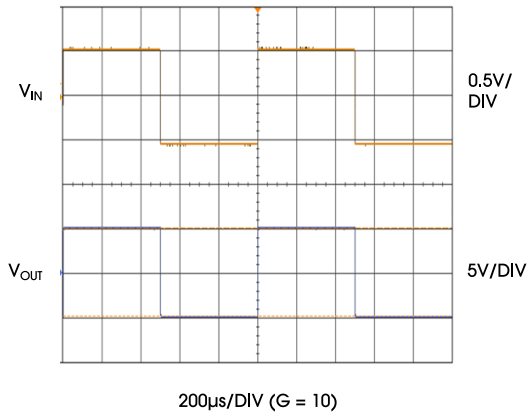


Figure 14. Large Signal Response (G = 10)

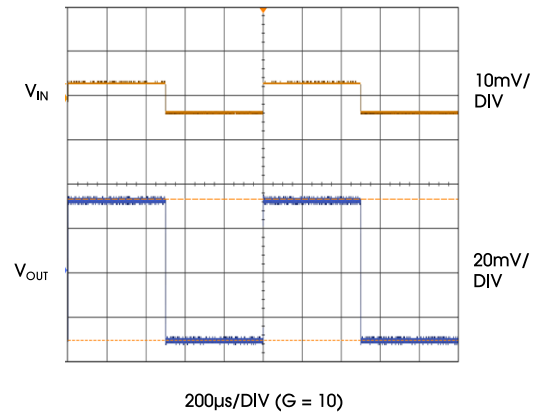


Figure 15. Small Signal Response (G = 10)

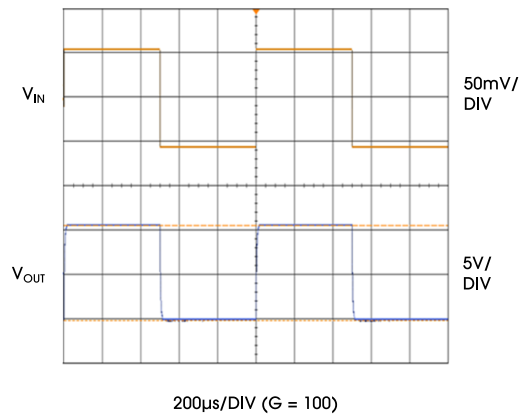


Figure 16. Large Signal Response (G = 100)

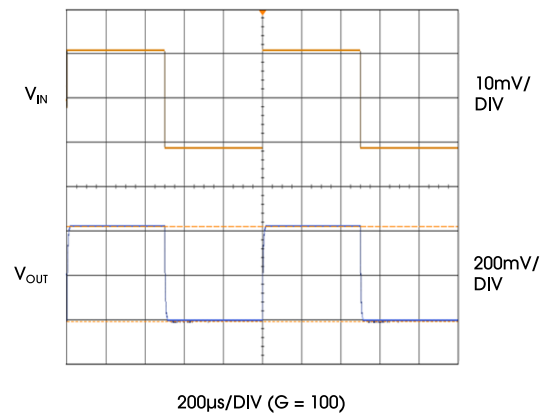


Figure 17. Small Signal Response (G = 100)

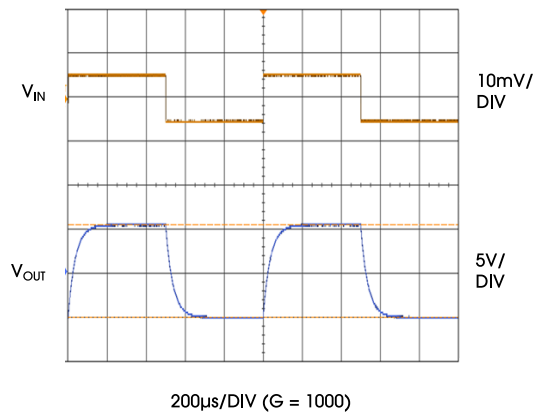


Figure 18. Large Signal Response (G = 1000)

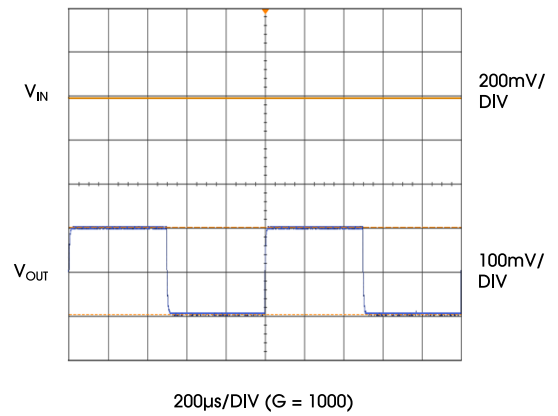


Figure 19. Small Signal Response (G = 1000)

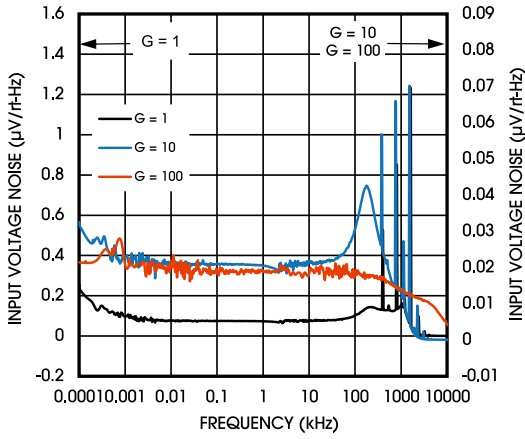


Figure 20. Input Voltage Noise Density

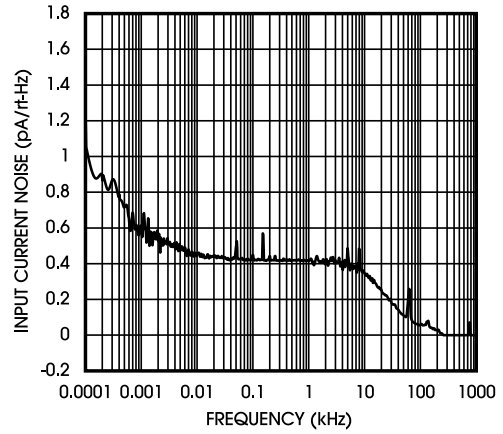


Figure 21. Input Current Noise Density

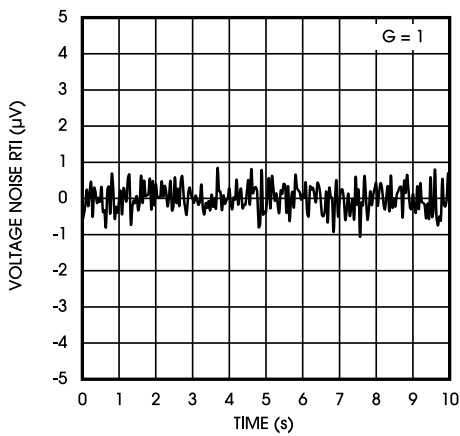


Figure 22. 0.1Hz to 10Hz RTI Voltage Noise

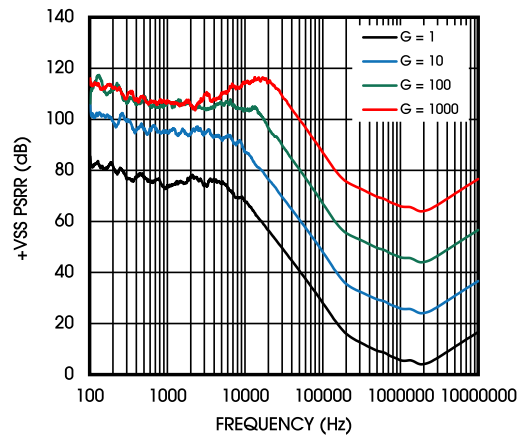


Figure 23. Positive PSRR vs. Frequency

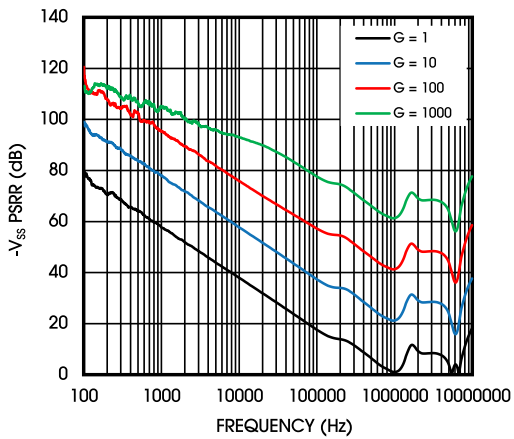


Figure 24. Negative PSRR vs. Frequency

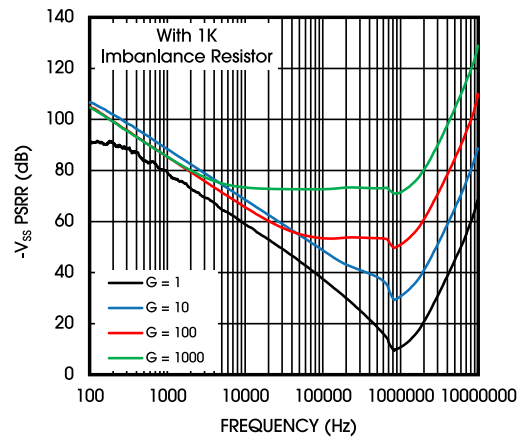


Figure 25. Imbalance CMRR vs. Frequency

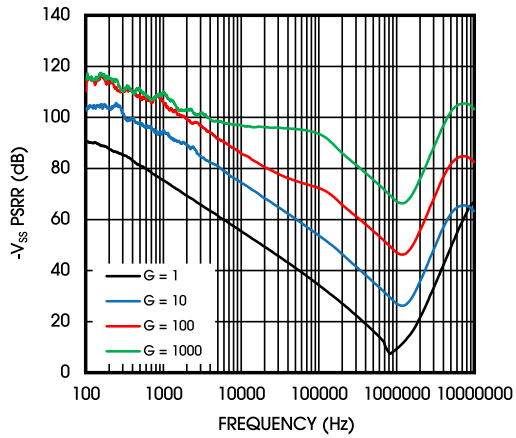


Figure 26. CMRR vs. Frequency

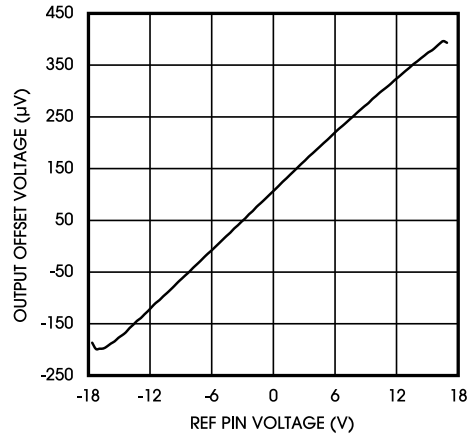


Figure 27. Reference Voltage vs. Output Offset Voltage

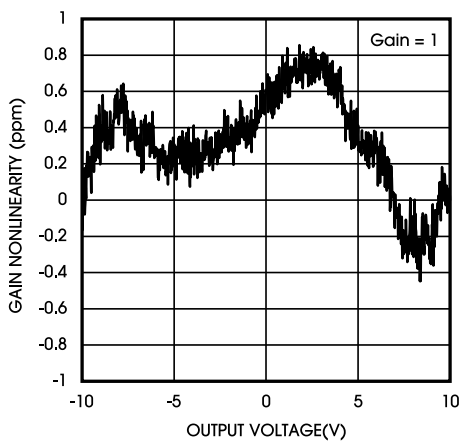


Figure 28. Gain Nonlinearity (G = 1)

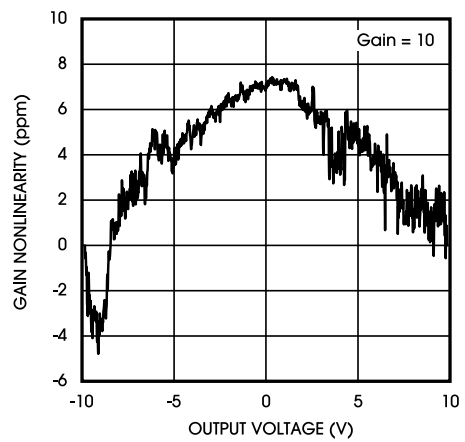


Figure 29. Gain Nonlinearity (G = 10)

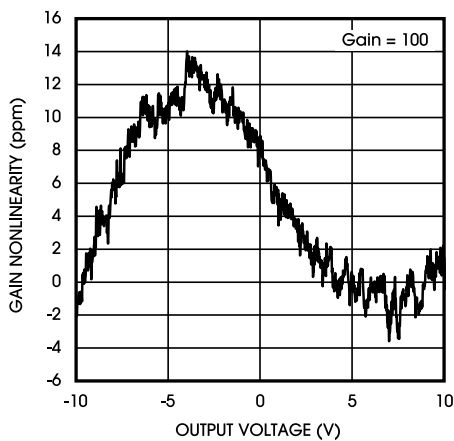


Figure 30. Gain Nonlinearity (G = 100)

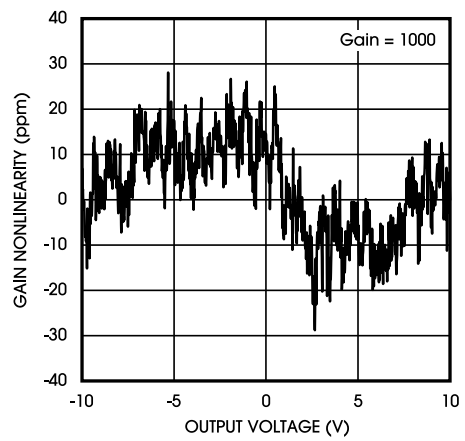


Figure 31. Gain Nonlinearity (G = 1000)

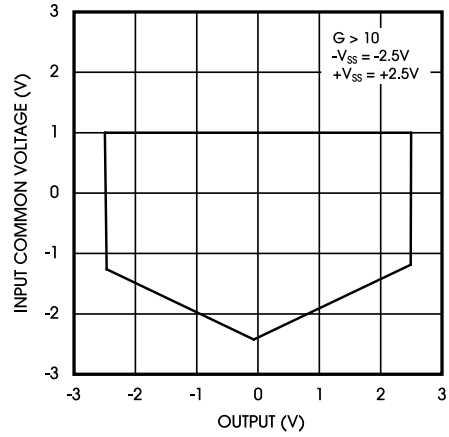
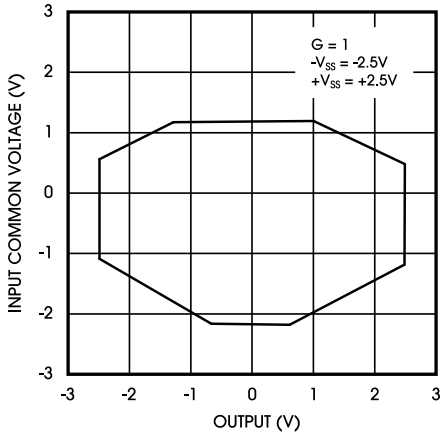


Figure 32. Input Common-Mode Range vs. Output Voltage,  $G = 1$  (5V)      Figure 33. Input Common-Mode Range vs. Output Voltage,  $G > 10$  (5V)

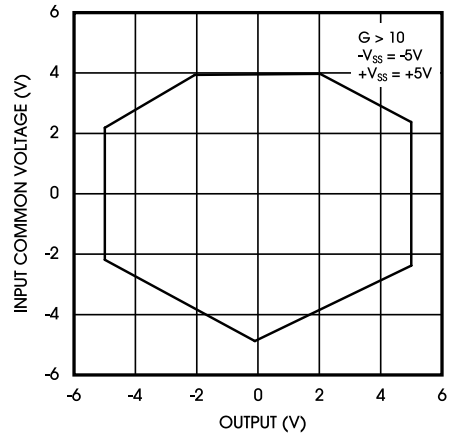
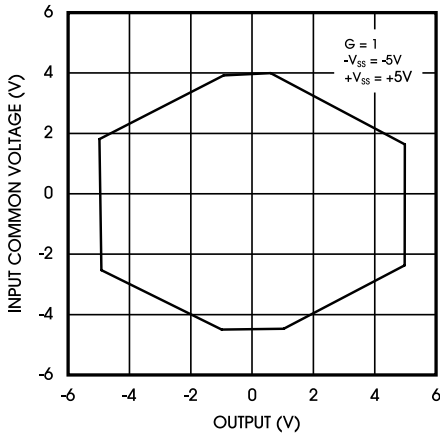


Figure 34. Input Common-Mode Range vs. Output Voltage,  $G = 1$  (10V)      Figure 35. Input Common-Mode Range vs. Output Voltage,  $G > 10$  (10V)

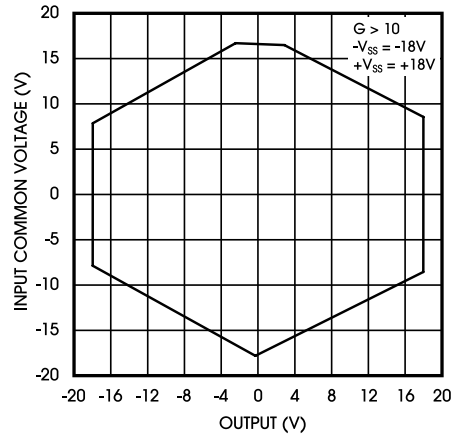
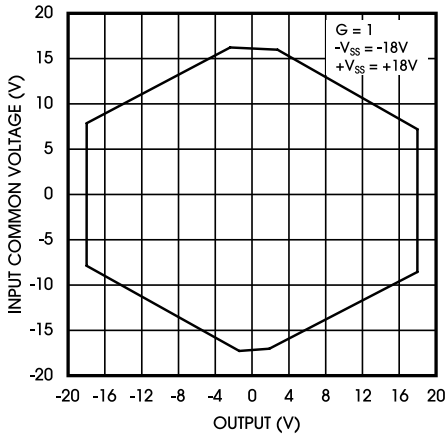


Figure 36. Input Common-Mode Range vs. Output Voltage,  $G = 1$  (36V)      Figure 37. Input Common-Mode Range vs. Output Voltage,  $G > 10$  (36V)

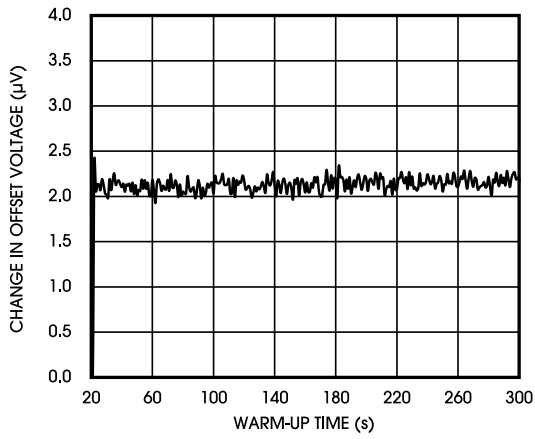


Figure 38. Warm-Up Time

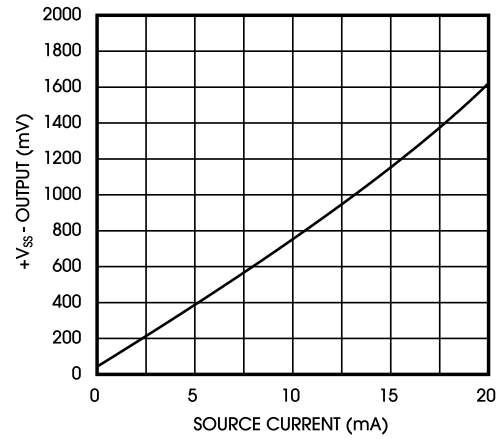


Figure 39.  $V_{OH}$  vs. Source Current

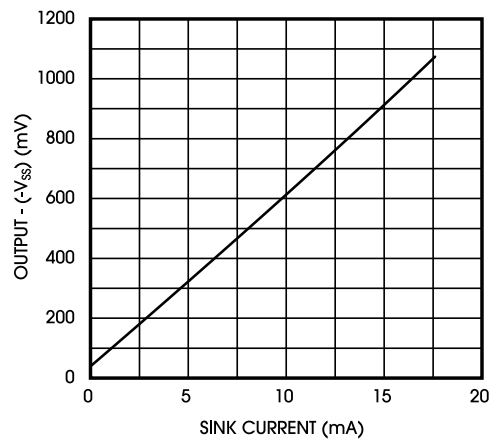


Figure 40.  $V_{OL}$  vs. Sink current

## 7. 详细说明

### 7.1 概述

INA103/INA104 是一款基于经典三运算放大器方法改进的单片仪表放大器。绝对值微调允许用户仅用一个电阻器就可以准确地对增益进行设置。单片结构和微调允许电路元件的紧密匹配和跟踪，从而确保该电路固有的高性能。

内部增益电阻器 R1 和 R2 被调整为 24.7kΩ 的绝对值，从而允许使用单个外部电阻器对增益进行精确编程。

那么增益方程为：

$$G = \frac{49.4k\Omega}{R_G} + 1 \quad (1)$$

$$R_G = \frac{49.4k\Omega}{G - 1} \quad (2)$$

作为参考 REF 引脚的单端输出，可将 REF 引脚连接到地或低电阻源。

### 7.2 功能模块框图

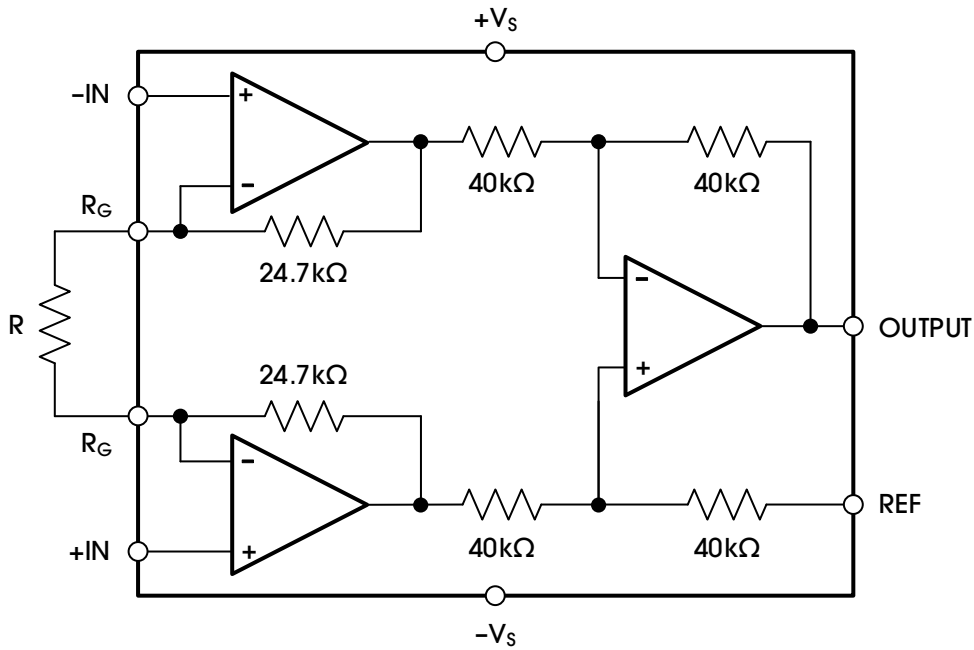


Figure 41. Functional Block Diagram

## 7.3 特性描述

### 7.3.1 精密 V-I 转换器

INA103/INA104 与另一个运算放大器和两个电阻器一起构成精密电流源(Figure 42)。运算放大器缓冲参考端子以保持良好的 CMR。INA103/INA104 的输出电压  $V_x$  出现在  $R_1$  两端，将其转换为电流。该电流，仅减去运算放大器的输入偏置电流，然后流出至负载。

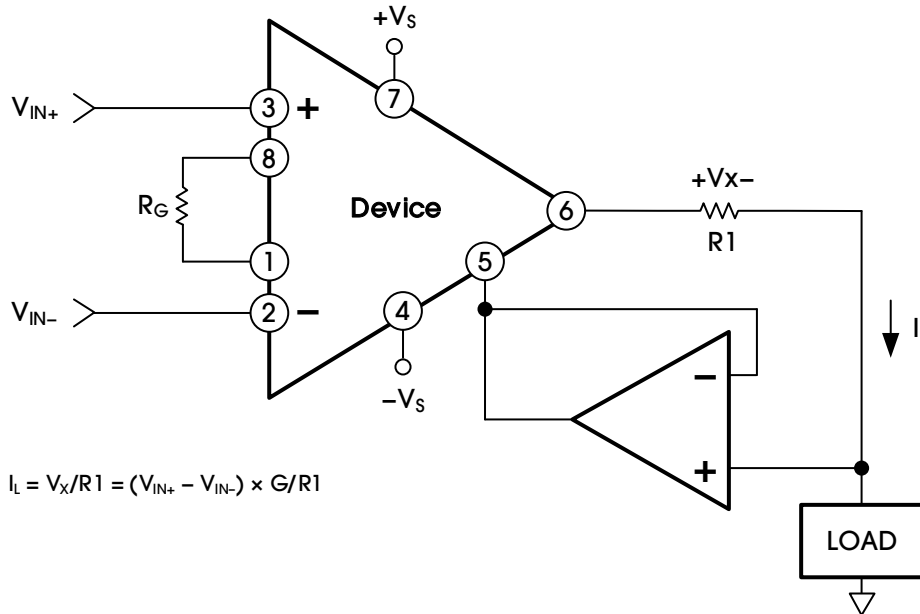


Figure 42. Precision Voltage-to-Current Converter

### 7.3.2 增益选择

INA103/INA104 增益由  $R_G$  电阻器编程，或更准确地说，由引脚 1 和 8 之间出现的任何阻抗进行设置。INA103/INA104 旨在使用 0.1% 至 1% 的电阻器提供精确增益。Table 9 显示了各种增益所需的  $R_G$  值。请注意，对于  $G = 1$ ， $R_G$  引脚未连接( $R_G = \infty$ )。对于任意增益，可以使用以下公式计算  $R_G$ ：

$$R_G = \frac{49.4k\Omega}{G - 1} \quad (3)$$

为了尽量减少增益误差，避免与  $R_G$  串联的高寄生电阻；为了最大限度地减少增益漂移， $R_G$  应具有较低的 TC——低于 10ppm/°C 以获得最佳性能。

Table 9. Required Values of Gain Resistors

1% STD TABLE VALUE OF $R_G$ ( $\Omega$ )	CALCULATED GAIN	0.1% STD TABLE VALUE OF $R_G$ ( $\Omega$ )	CALCULATED GAIN
49.9k	1.990	49.3k	2.002
12.4k	4.984	12.4k	4.984
5.49k	9.998	5.49k	9.998
2.61k	19.93	2.61k	19.93
1.00k	50.40	1.01k	49.91
499	100.0	499	100.0
249	199.4	249	199.4
100	495.0	98.8	501.0
49.9	991.0	49.3	1,003.0

### 7.3.3 输入和输出失调电压

INA103/INA104 的低误差归因于两个来源，输入和输出误差。当参考输入时，输出误差除以  $G$ 。实际上，输入误差在高增益时占主导地位，而输出误差在低增益时占主导地位。给定增益的总  $V_{OS}$  计算如下：

$$\text{Total Error RTI} = \text{Input Error} + (\text{Output Error} / G) \quad (4)$$

$$\text{Total Error RTO} = (\text{Input Error} \times G) + \text{Output Error} \quad (5)$$

### 7.3.4 参考终端

参考端子电位定义了零输出电压，当负载不与系统的其余部分共享精确接地时尤其有用。它提供了一种向输出注入精确偏移的直接方法。为获得最佳  $CMR$ ，寄生电阻应保持在最低水平。

### 7.3.5 输入保护

对于超出电源的输入电压，应在每个输入端串联一个保护电阻器，以将电流限制在  $10\text{mA}$ 。这些可以是与  $RFI$  滤波器中使用的电阻器相同的电阻器。高电阻值会影响系统的噪声和交流  $CMRR$  性能。可以在输入端放置低漏电二极管(例如  $BAV199$ )以降低所需的保护电阻。

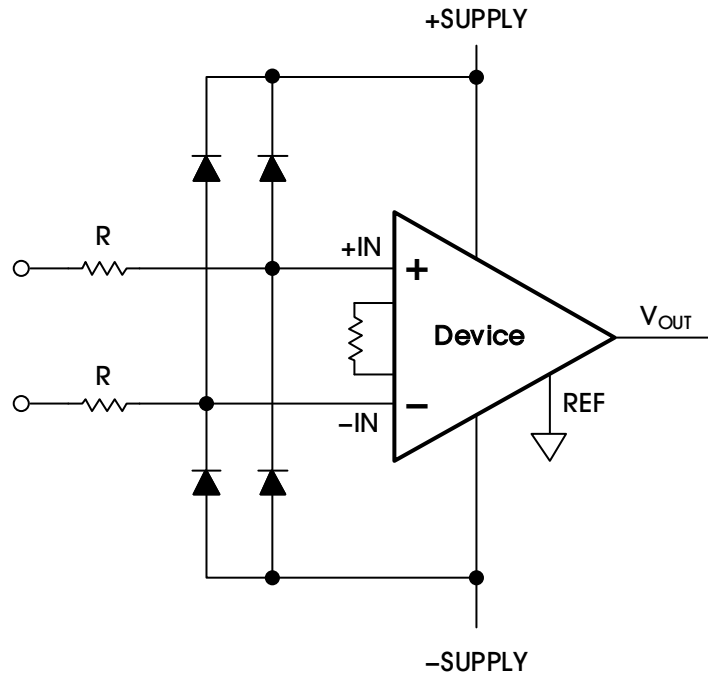


Figure 43. Diode Protection for Voltages Beyond Supply

### 7.3.6 射频干扰

所有仪表放大器都会对小的带外信号进行整流。干扰可能表现为一个小的直流电压偏移。可以使用放置在仪表放大器输入端的低通 R-C 网络过滤高频信号。Figure 44 展示了这样的配置。滤波器根据以下关系限制输入信号：

$$\text{FilterFreq}_{\text{DIFF}} = \frac{1}{2\pi R(2C_D + C_C)} \quad (6)$$

$$\text{FilterFreq}_{\text{CM}} = \frac{1}{2\pi RC_C} \quad (7)$$

其中：

- $C_D \geq 10C_C$ .

$C_D$  影响差值信号。 $C_C$  影响共模信号。 $R \times C_C$  的任何不匹配都会降低 INA103/INA104 CMRR。为避免无意中降低 CMRR 带宽性能，请确保  $C_C$  至少比  $C_D$  小一个数量级。不匹配的  $C_C$  的影响随着  $C_D:C_C$  比率的增加而降低。

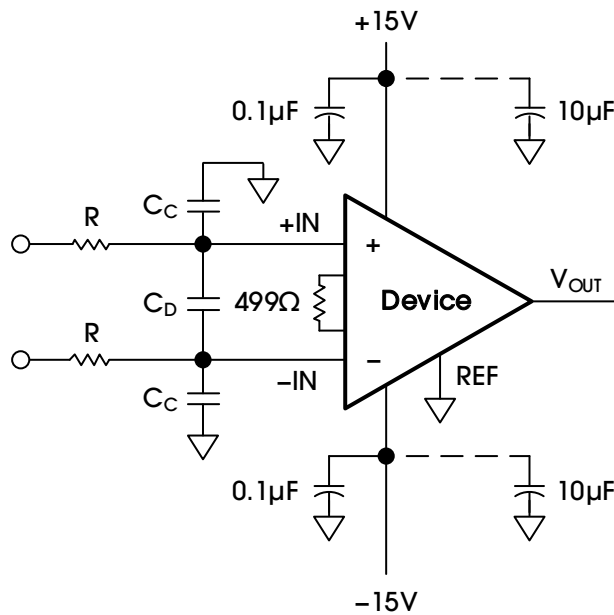


Figure 44. Circuit to Attenuate RF Interference

### 7.3.7 共模抑制

INA103/INA104 仪表放大器提供高 CMR，这是衡量两个输入等量变化时输出电压变化的指标。这些规格通常针对全范围输入电压变化和指定的源不平衡给出。

为获得最佳 CMR，参考端子应连接到低阻抗点，并且两个输入之间的电容和电阻差异应保持在最小值。在许多应用中，屏蔽电缆被用于最小化噪声；为了在频率范围内获得最佳 CMR，应正确驱动屏蔽。Figure 45 和 Figure 46 显示了有源数据保护，它们被配置为通过“自举”输入电缆屏蔽层的电容来提高交流共模抑制，从而最大限度地减少输入之间的电容失配。

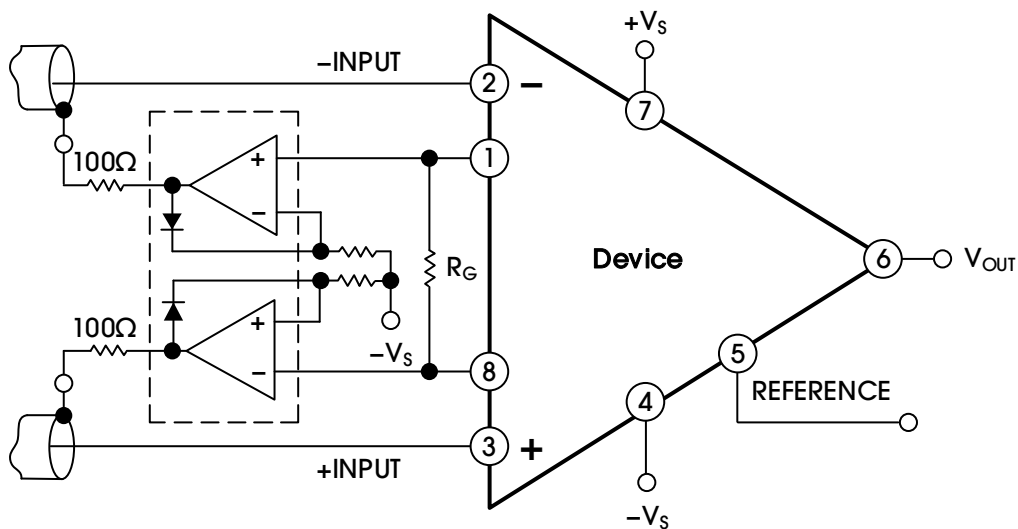


Figure 45. Differential Shield Driver

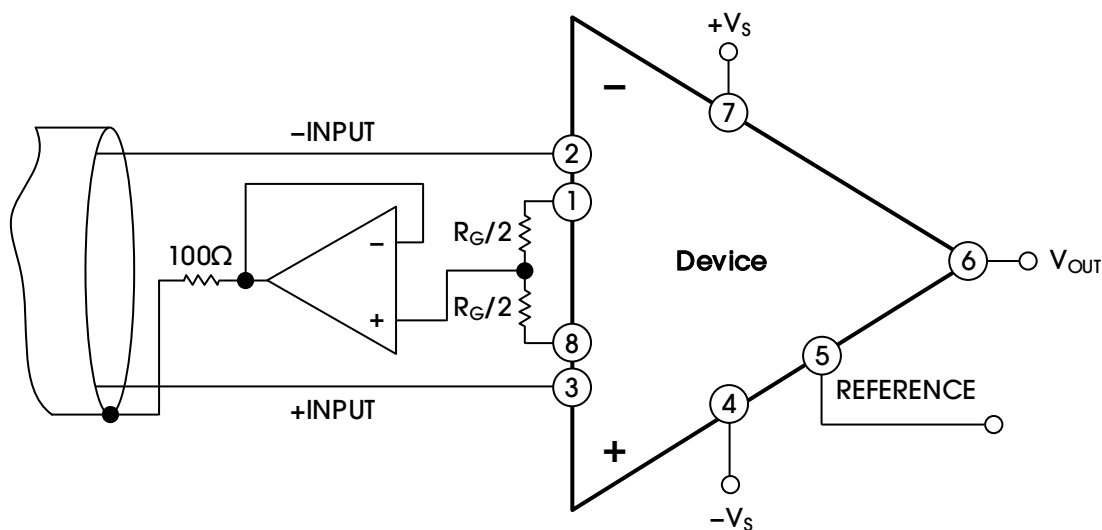


Figure 46. Common-Mode Shield Driver

### 7.3.8 共模输入范围

INA103/INA104 输入电路的线性输入电压范围比正电压低大约 2V，比负电源高 0.1V。差分输入电压导致输出电压增加；但是，线性输入范围受限于放大器的输入级输出电压摆幅。因此，线性共模输入范围与整个放大器的输出电压有关。这种行为也取决于电源电压。输入过载会产生看似正常的输出电压。例如，如果输入过载条件将两个输入放大器驱动到它们的正输出摆幅限制，由输出测量的差分电压放大器接近于零。输出级输出接近 0V，即使两个输入都过载。可以参见 Figure 32 至 Figure 37。

### 7.3.9 输入偏置电流的接地回路

输入偏置电流是偏置放大器输入晶体管所必需的电流。这些电流必须有直接返回路径。因此，当放大“浮动”输入源(例如变压器或交流耦合源)时，每个输入到地之间必须有一条直流路径，如 Figure 47、Figure 48 和 Figure 49 所示。

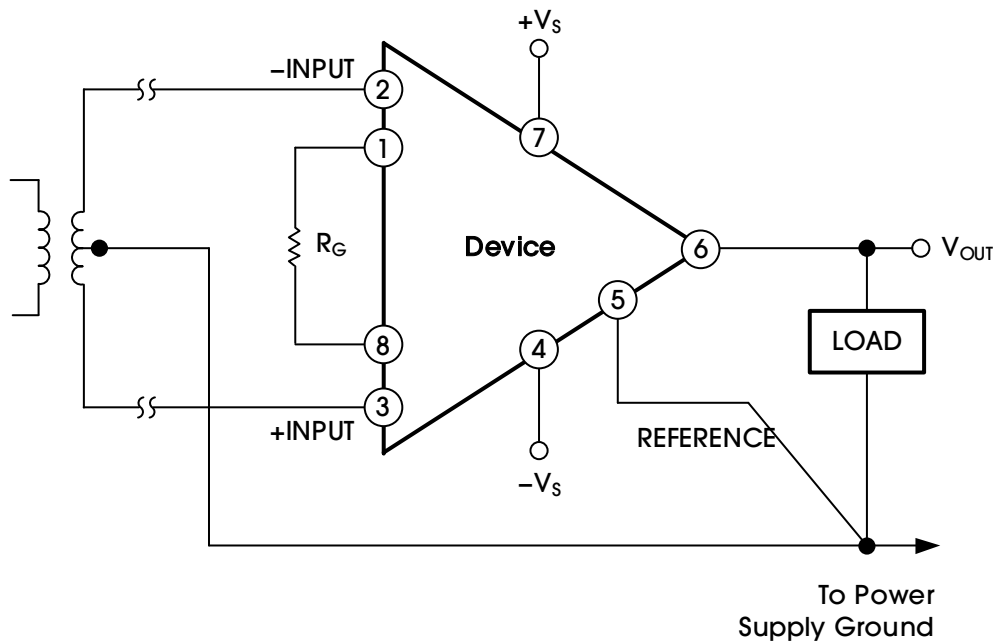


Figure 47. Ground Returns for Bias Currents with Transformer-Coupled Inputs

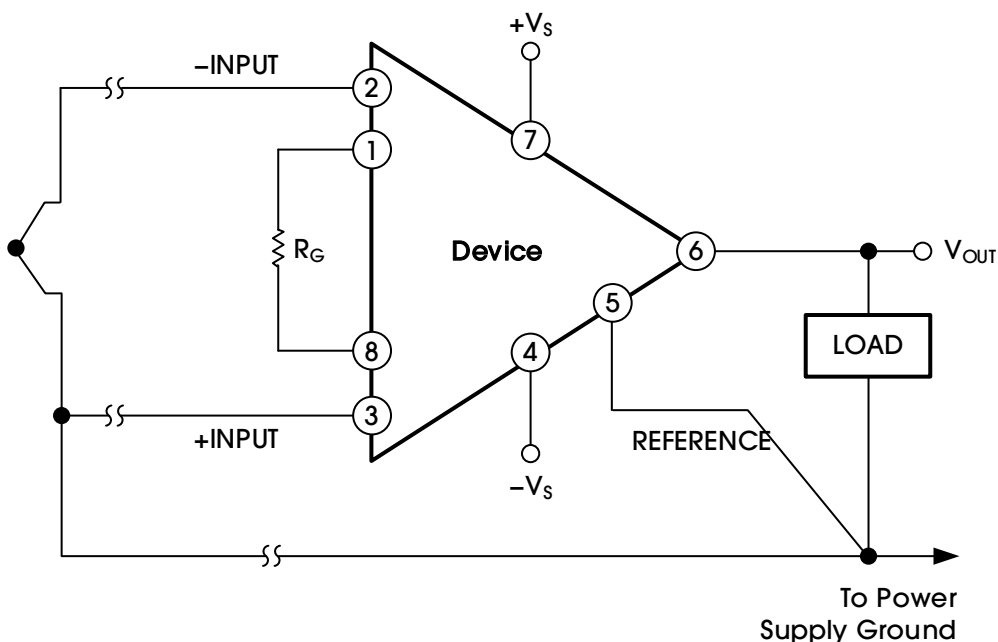


Figure 48. Ground Returns for Bias Currents with Thermocouple Inputs

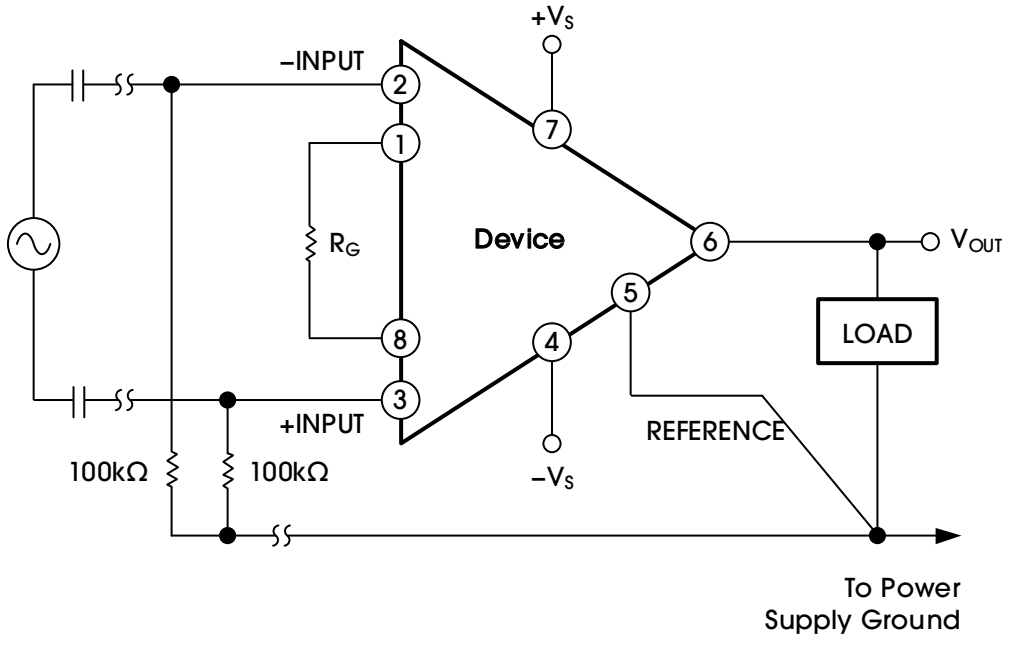


Figure 49. Ground Returns for Bias Currents with AC-Coupled Inputs

## 8. PACKAGE INFORMATION

The INA103/INA104 is available in the MSOP-8 and SOIC-8 packages.

### 8.1 MSOP-8 PACKAGE

Figure 50 shows the MSOP-8 package view.

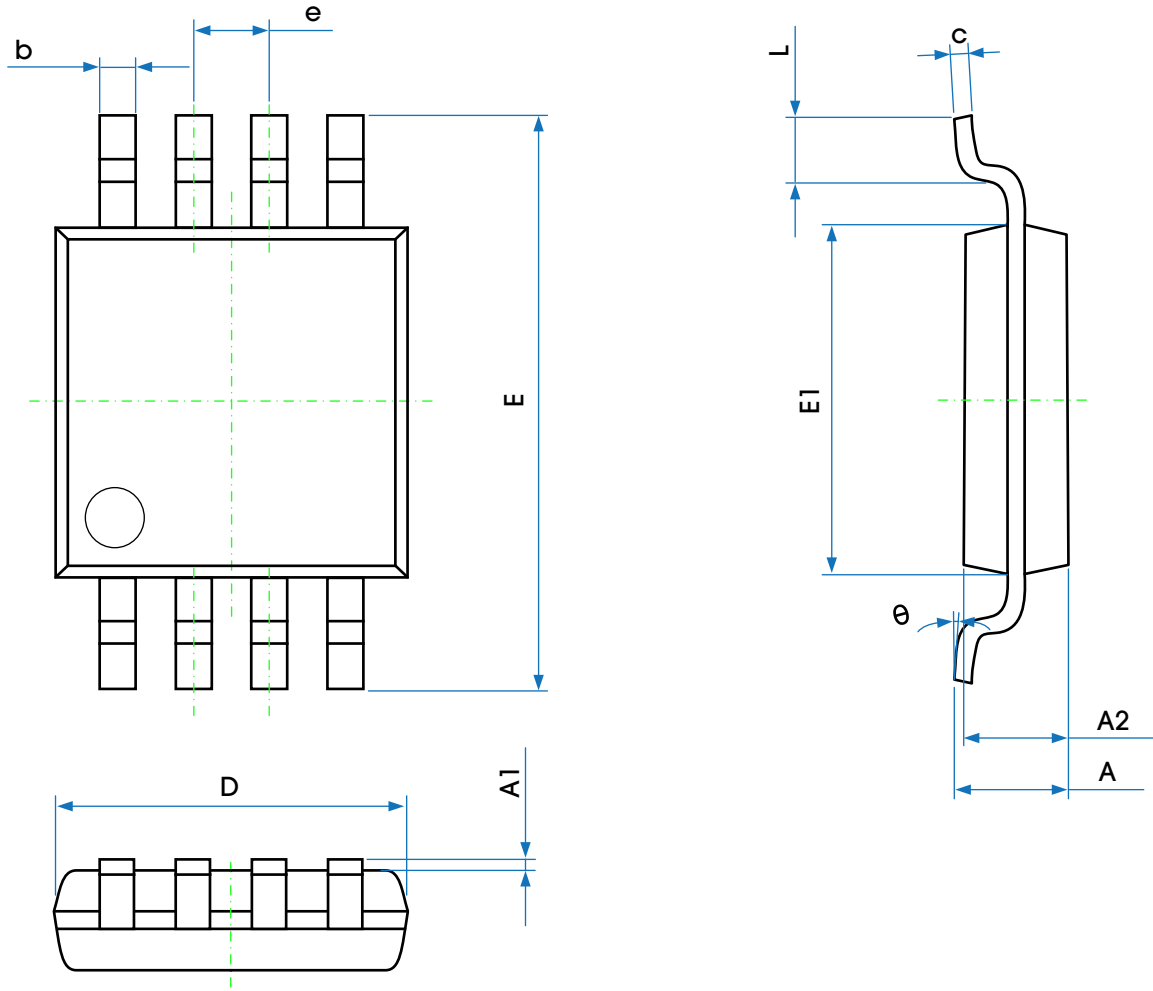


Figure 50. MSOP-8 Package View

Table 10 provides detailed information about the dimensions of the MSOP-8 package.

Table 10. Dimensions of the MSOP-8 Package

SYMBOL	DIMENSIONS IN MILLIMETERS		DIMENSIONS IN INCHES	
	MIN	MAX	MIN	MAX
A	—	1.100	—	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.250	0.380	0.010	0.015
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
e	0.650 (BSC)		0.026 (BSC)	
E	4.750	5.050	0.187	0.199
E1	2.900	3.100	0.114	0.122
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

## 8.2 SOIC-8 PACKAGE

Figure 51 shows the SOIC-8 package view.

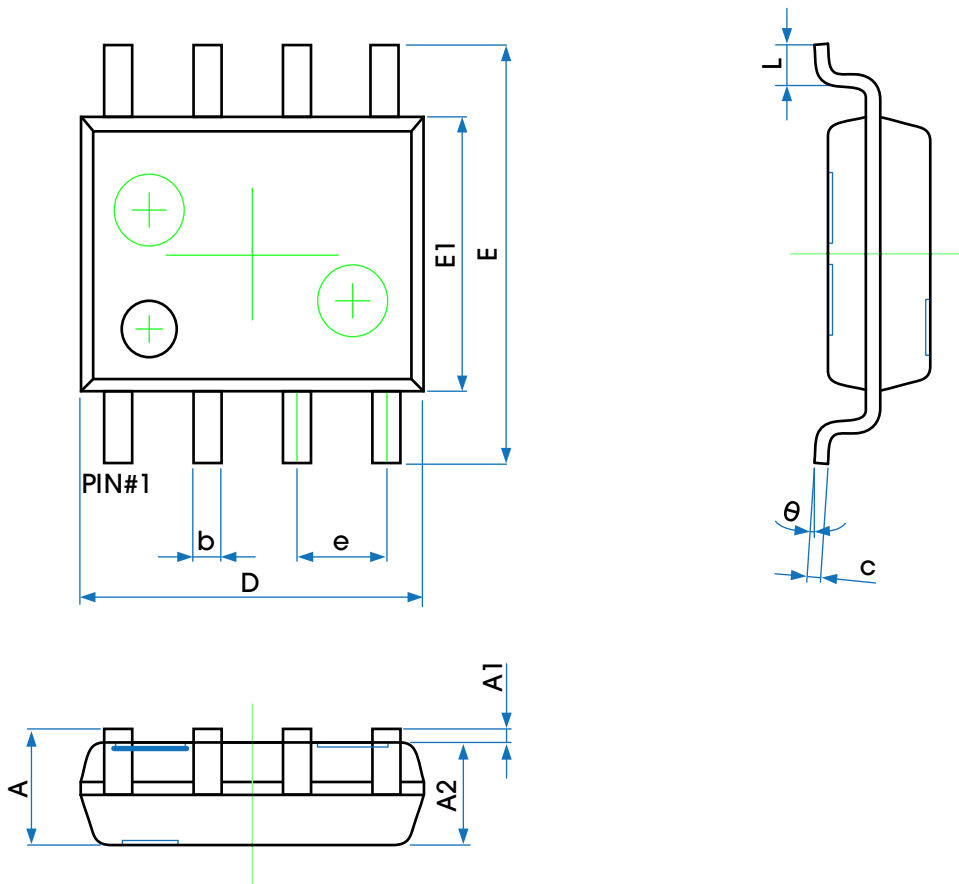


Figure 51. SOIC-8 Package View

Table 11 provides detailed information about the dimensions of the SOIC-8 package.

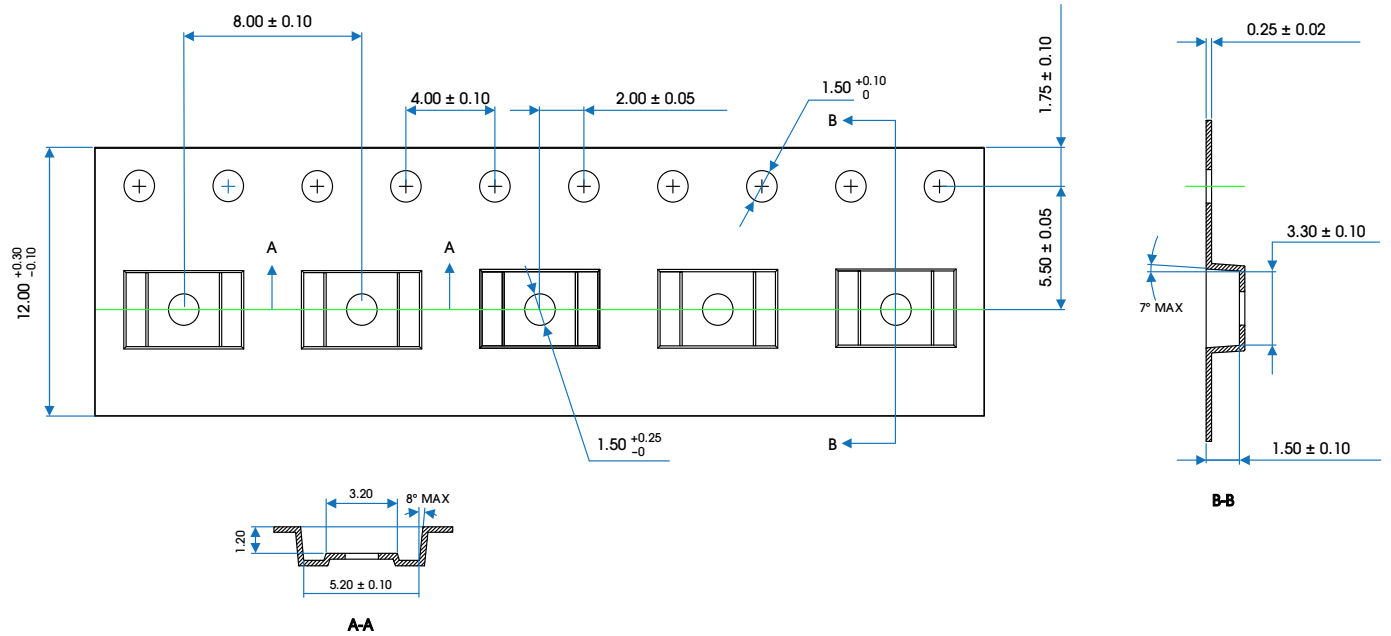
Table 11. Dimensions of the SOIC-8 Package

SYMBOL	DIMENSIONS IN MILLIMETERS		DIMENSIONS IN INCHES	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
$\theta$	0°	8°	0°	8°

## 9. TAPE AND REEL INFORMATION

### 9.1 MSOP-8 PACKAGE

Figure 52 illustrates the carrier tape of the MSOP-8 package.



**Notes:**

1. Cover tape width:  $9.5 \pm 0.10$ .
2. Cumulative tolerance of 10 sprocket hole pitch:  $\pm 0.20$  (max).
3. Camber: not to exceed 1mm in 100mm.
4. Mold#: MSOP-8.
5. All dimensions: mm.
6. Direction of view:

Figure 52. Carrier Tape Drawing (MSOP-8 Package)

Table 12 provides information about tape and reel (MSOP-8 Package).

Table 12. Tape and Reel Information (MSOP-8 Package)

PACKAGE TYPE	REEL	QTY/REEL	REEL/ INNER BOX	INNER BOX/ CARTON	QTY/CARTON	INNER BOX SIZE (mm)	CARTON SIZE (mm)
MSOP-8	13"	4000	1	8	32000	358*340*50	430*380*390

Figure 53 shows the product loading orientation—pin 1 is assigned at Q1.

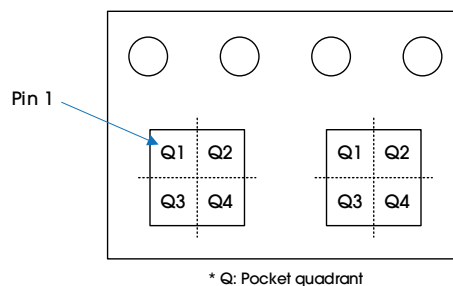
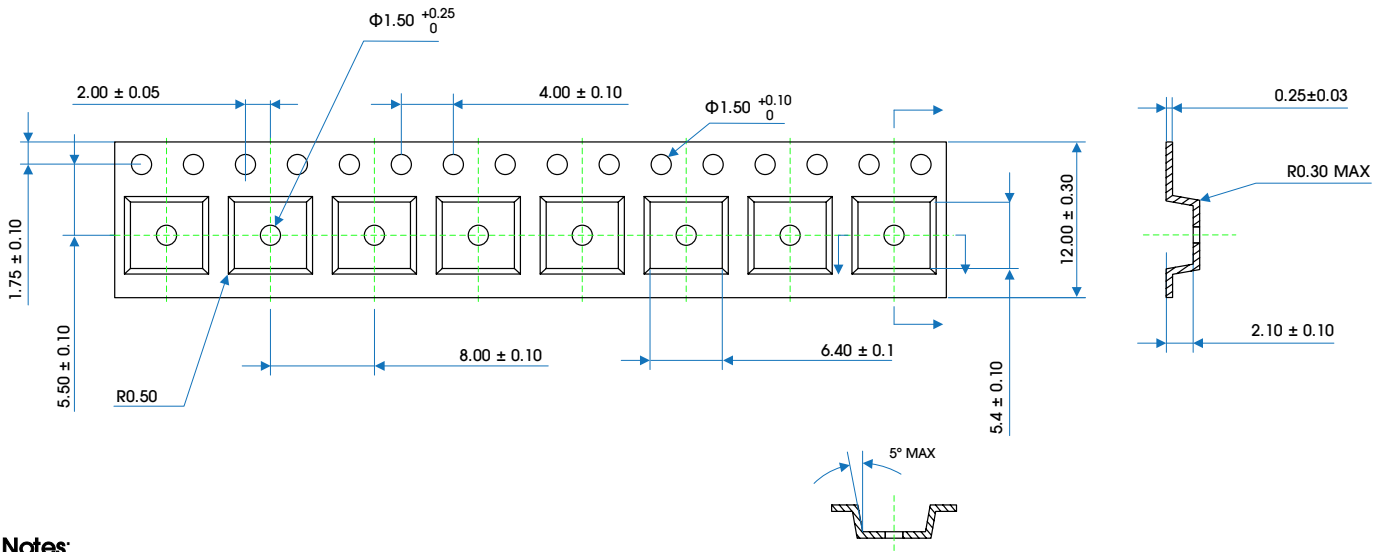


Figure 53. Product Loading Orientation

## 9.2 SOIC-8 PACKAGE

Figure 54 illustrates the carrier tape of the SOIC-8 package.



**Notes:**

1. Cover tape width:  $9.5 \pm 0.10$ .
2. Cumulative tolerance of 10 sprocket hole pitch:  $\pm 0.20$  (max).
3. Camber: not to exceed 1mm in 100mm.
4. Mold#: SOIC-8.
5. All dimensions: mm.
6. Direction of view:

Figure 54. Carrier Tape Drawing (SOIC-8 Package)

Table 13 provides information about tape and reel (SOIC-8 Package).

Table 13. Tape and Reel Information (SOIC-8 Package)

PACKAGE TYPE	REEL	QTY/REEL	REEL/ INNER BOX	INNER BOX/ CARTON	QTY/CARTON	INNER BOX SIZE (mm)	CARTON SIZE (mm)
SOIC-8	13"	4000	1	8	32000	358*340*50	430*380*390

Figure 55 shows the product loading orientation—pin 1 is assigned at Q1.

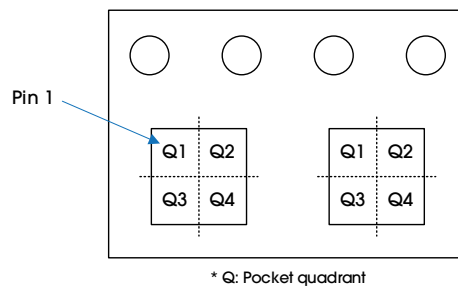


Figure 55. Product Loading Orientation

## REVISION HISTORY

REVISION	DATE	DESCRIPTION
Rev A	30 August 2023	Rev A release.
Rev B	26 August 204	Updated the values related with common-mode rejection in Table 8.