

BLF8G20LS-400PV; BLF8G20LS-400PGV

Power LDMOS transistor

Rev. 1 — 6 June 2013

Preliminary data sheet

1. Product profile

1.1 General description

400 W LDMOS power transistor with improved video bandwidth for base station applications at frequencies from 1805 MHz to 1995 MHz.

Table 1. Typical performance

Typical RF performance at $T_{case} = 25\text{ °C}$ in a common source class-AB production test circuit, tested on straight lead device.

Test signal	f (MHz)	I_{Dq} (mA)	V_{DS} (V)	$P_{L(AV)}$ (W)	G_p (dB)	η_D (%)	ACPR _{5M} (dBc)
2-carrier W-CDMA	1805 to 1995	3400	28	95	19	28	-33 [1]

[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 7.5 dB at 0.01 % probability on CCDF; carrier spacing = 5 MHz; $f_1 = 1807.5\text{ MHz}$; $f_2 = 1812.5\text{ MHz}$; $f_3 = 1872.5\text{ MHz}$; $f_4 = 1877.5\text{ MHz}$.

1.2 Features and benefits

- Decoupling leads to enable improved Video BandWidth (VBW) (120 MHz typical)
- High efficiency
- Low R_{th} providing excellent thermal stability
- Designed for broadband operation
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Design optimized for gull-wing
- Excellent ruggedness
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 1805 MHz to 1995 MHz frequency range



2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF8G20LS-400PV (SOT1242B)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source		
6	decoupling1		
7	decoupling2		
8	n.c.		
9	n.c.		
BLF8G20LS-400PGV (SOT1242C)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source		
6	decoupling1		
7	decoupling2		
8	n.c.		
9	n.c.		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BLF8G20LS-400PV	-	earless flanged ceramic package; 8 leads	SOT1242B
BLF8G20LS-400PGV	-	earless flanged ceramic package; 8 leads	SOT1242C

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+13	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		[1]	225	°C

[1] Continuous use at maximum temperature will affect the reliability.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}$; $P_L = 80\text{ W}$	0.23	K/W

6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ °C}$; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 3.0\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 300\text{ mA}$	1.5	1.9	2.3	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}$; $V_{DS} = 28\text{ V}$	-	-	3.0	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $V_{DS} = 10\text{ V}$	-	51.5	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}$; $V_{DS} = 0\text{ V}$	-	-	300	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}$; $I_D = 15\text{ A}$	-	20.6	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$; $I_D = 10.5\text{ A}$	-	0.055	-	Ω

Table 7. RF characteristics

Test signal: 2-carrier W-CDMA; PAR = 7.5 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1-64 DPCH; $f_1 = 1807.5\text{ MHz}$; $f_2 = 1812.5\text{ MHz}$; $f_3 = 1872.5\text{ MHz}$; $f_4 = 1877.5\text{ MHz}$; RF performance at $V_{DS} = 28\text{ V}$; $I_{Dq} = 3400\text{ mA}$; $T_{case} = 25\text{ °C}$; unless otherwise specified; in a class-AB production test circuit, tested on straight lead device.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)} = 95\text{ W}$	17.8	19	-	dB
RL_{in}	input return loss	$P_{L(AV)} = 95\text{ W}$	-	-12	-6	dB
η_D	drain efficiency	$P_{L(AV)} = 95\text{ W}$	24	28	-	%
$ACPR_{5M}$	adjacent channel power ratio (5 MHz)	$P_{L(AV)} = 95\text{ W}$	-	-33	-28	dBc

7. Test information

7.1 Ruggedness in class-AB operation

The BLF8G20LS-400PV and BLF8G20LS-400PGV are capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: $V_{DS} = 28\text{ V}$; $I_{DQ} = 3300\text{ mA}$; 2-carrier W-CDMA signal; $P_L = 200\text{ W}$; $f_c = 1800\text{ MHz}$; 5 MHz spacing, 46 % clipping.

7.2 Impedance information

Table 8. Typical impedance for the top-half of the push-pull package

Measured load-pull data; $I_{DQ} = 1800\text{ mA}$; $V_{DS} = 28\text{ V}$; $T_{case} = 25\text{ °C}$, water cooled.

f (MHz)	Z_S ^[1] (Ω)	Z_L ^[1] (Ω)
BLF8G20LS-400PV (straight lead)		
1800	4.1 – j4.66	4.1 – j4.5
1840	5.2 – j3.6	4.4 – j4.4
1880	4.6 – j1.45	4.85 – j4.25
1930	2.8 – j0.3	4.5 – j4.3
1960	2.1 – j0.5	5.5 – j3.5
1990	1.56 – j0.6	5.5 – j3.4
BLF8G20LS-400PGV (gull-wing)		
1800	3.7 – j7.6	4.2 – j6.8
1840	4.34 – j6.1	4.4 – j6.7
1880	4.75 – j5.2	4 – j6.4
1930	3.17 – j3.4	4.6 – j6.5
1960	2 – j3.05	5.8 – j5.5
1990	2.5 – j2.6	5.8 – j5.7

[1] Z_S and Z_L defined in [Figure 1](#).

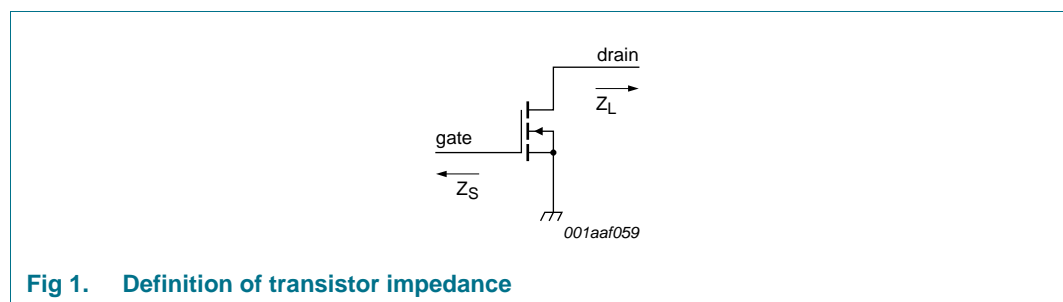


Fig 1. Definition of transistor impedance

7.3 VBW in class-AB operation

The BLF8G20LS-400PV and BLF8G20LS-400PGV have a video bandwidth of 120 MHz (typical) when measured in a class-AB test circuit operating in the 1800 MHz to 1880 MHz frequency band for $V_{DS} = 28\text{ V}$ and $I_{DQ} = 3.3\text{ A}$, where the VBW is defined as the location of the resonance in the base-band impedance measurement obtained using a low-frequency probe.

The VBW measurement based on the 2-tone IMD test as a function of carrier spacing is shown below.

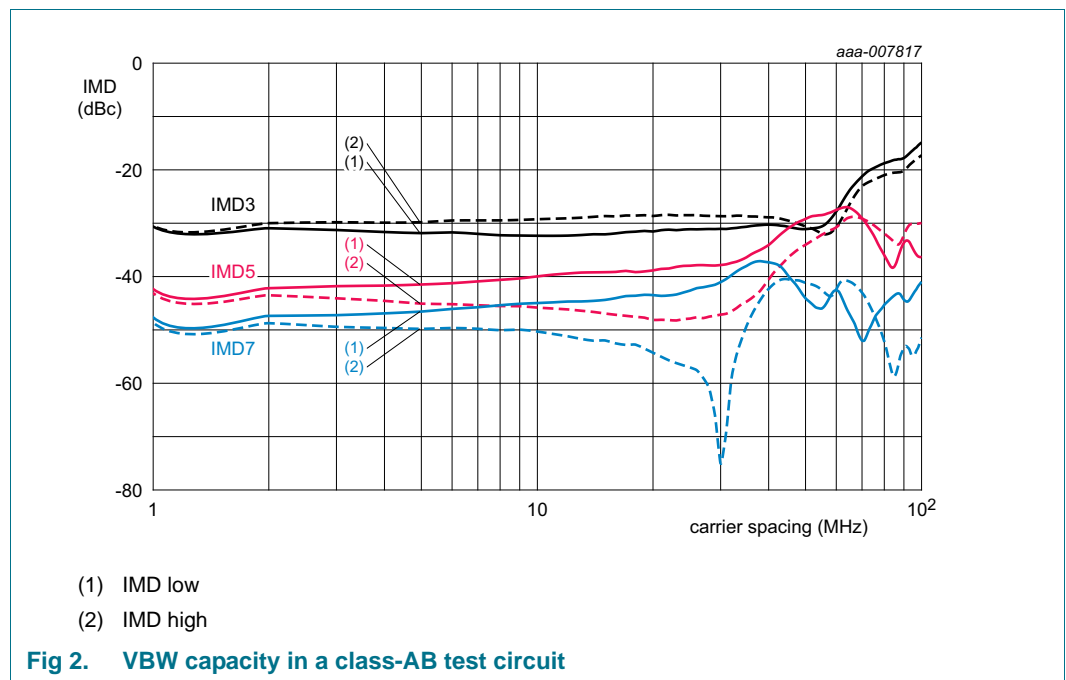


Fig 2. VBW capacity in a class-AB test circuit

7.4 Test circuit

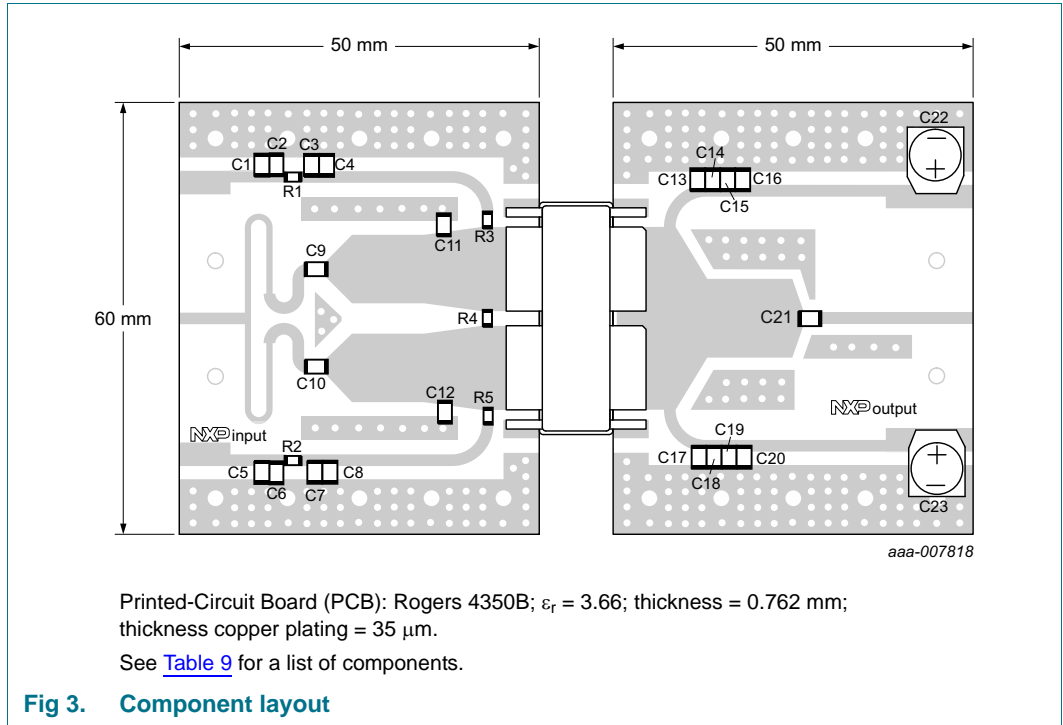


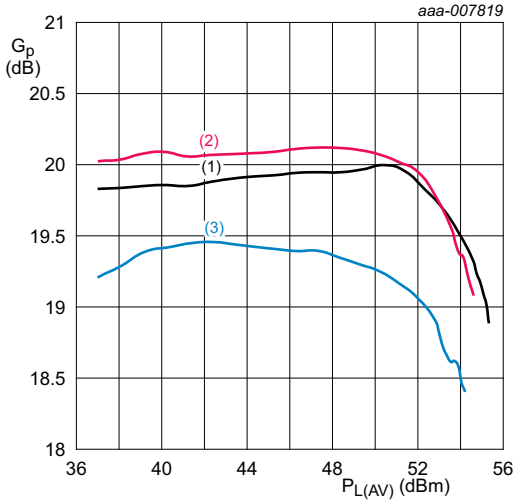
Table 9. List of components

See [Figure 3](#) for component layout.

Component	Description	Value	Remarks
C1, C5, C16, C20	multilayer ceramic chip capacitor	10 μF , 50 V	Murata, SMD 2220
C2, C6, C15, C19	multilayer ceramic chip capacitor	4.7 μF , 50 V	Murata
C3, C7, C14, C18	multilayer ceramic chip capacitor	1 nF	ATC100B
C4, C8, C9, C10, C13, C17, C21	multilayer ceramic chip capacitor	24 pF	ATC100B
C11, C12	multilayer ceramic chip capacitor	100 pF	ATC100B
C22, C23	electrolytic capacitor	2200 μF , 63 V	
R1, R2	resistor	10 Ω	SMD 1206
R3, R5	resistor	5.1 Ω	SMD 1206
R4	resistor	33 Ω	SMD 1206

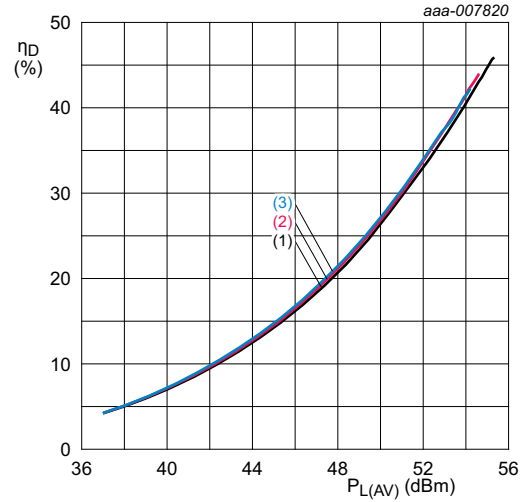
7.5 Graphical data

7.5.1 CW



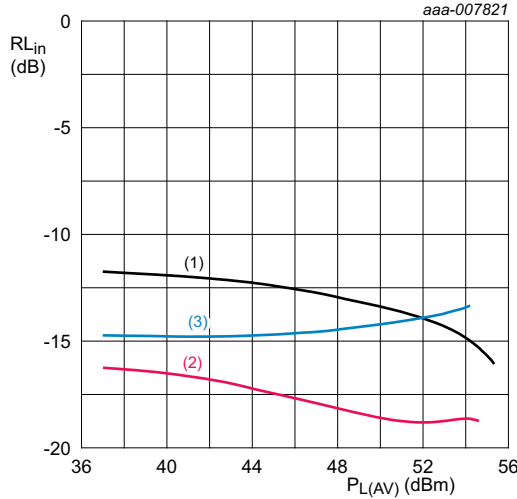
$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA.}$
 (1) $f = 1805\text{ MHz}$
 (2) $f = 1840\text{ MHz}$
 (3) $f = 1880\text{ MHz}$

Fig 4. Power gain as a function of average output power; typical values



$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA.}$
 (1) $f = 1805\text{ MHz}$
 (2) $f = 1840\text{ MHz}$
 (3) $f = 1880\text{ MHz}$

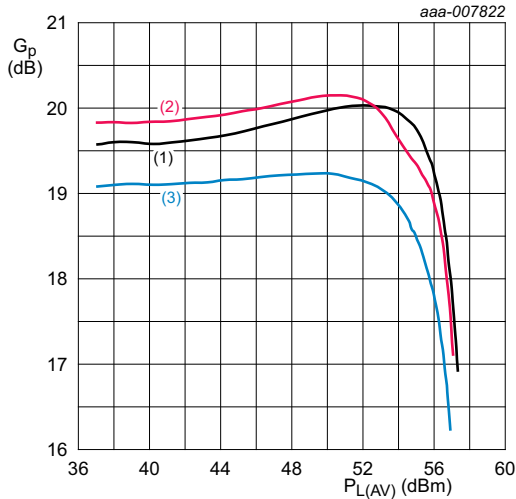
Fig 5. Drain efficiency as a function of average output power; typical values



$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA.}$
 (1) $f = 1805\text{ MHz}$
 (2) $f = 1840\text{ MHz}$
 (3) $f = 1880\text{ MHz}$

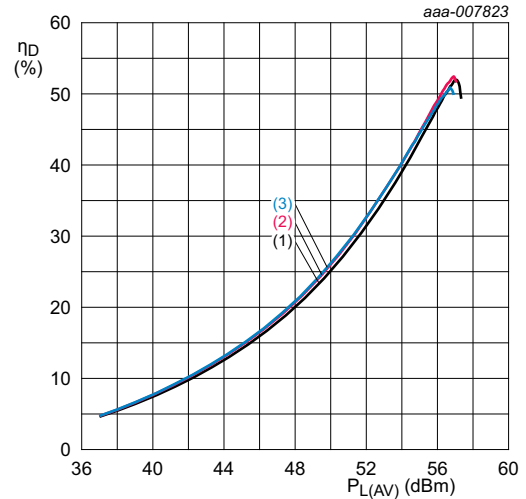
Fig 6. Input return loss as a function of average output power; typical values

7.5.2 Pulsed CW



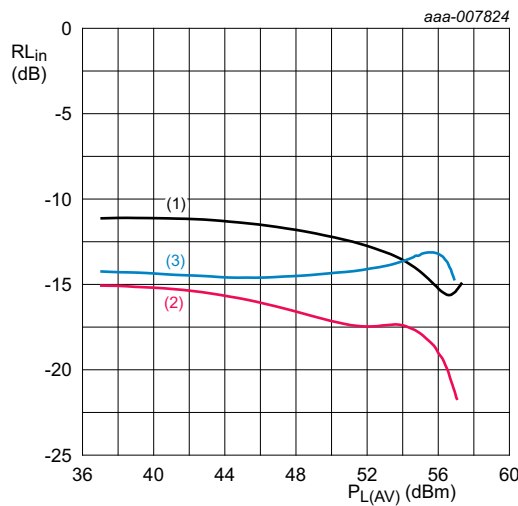
$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA}.$
 (1) $f = 1805\text{ MHz}$
 (2) $f = 1840\text{ MHz}$
 (3) $f = 1880\text{ MHz}$

Fig 7. Power gain as a function of average output power; typical values



$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA}.$
 (1) $f = 1805\text{ MHz}$
 (2) $f = 1840\text{ MHz}$
 (3) $f = 1880\text{ MHz}$

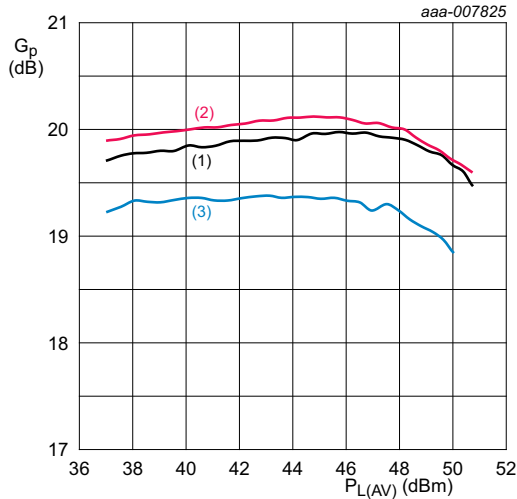
Fig 8. Drain efficiency as a function of average output power; typical values



$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA}.$
 (1) $f = 1805\text{ MHz}$
 (2) $f = 1840\text{ MHz}$
 (3) $f = 1880\text{ MHz}$

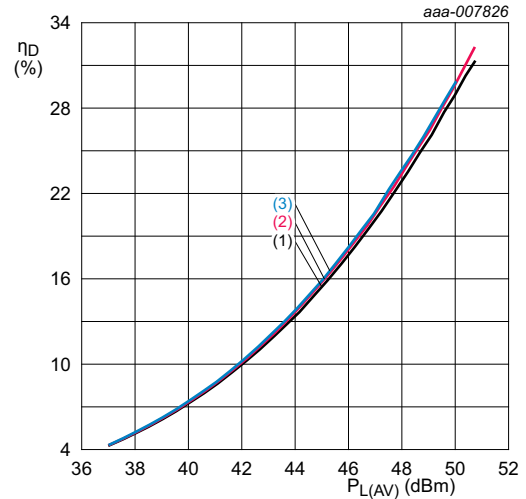
Fig 9. Input return loss as a function of average output power; typical values

7.5.3 IS-95



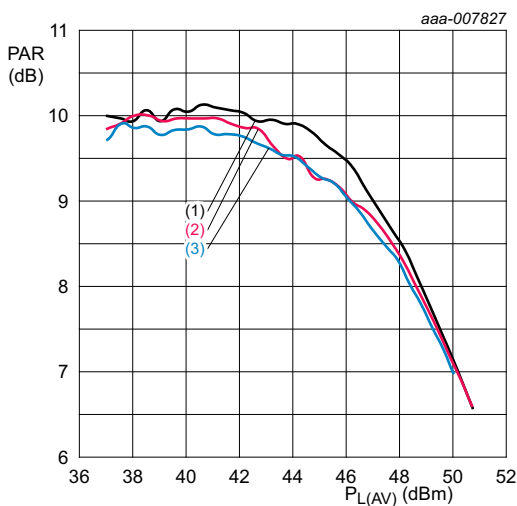
$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA}.$
 (1) $f = 1805\text{ MHz}$
 (2) $f = 1840\text{ MHz}$
 (3) $f = 1880\text{ MHz}$

Fig 10. Power gain as a function of average output power; typical values



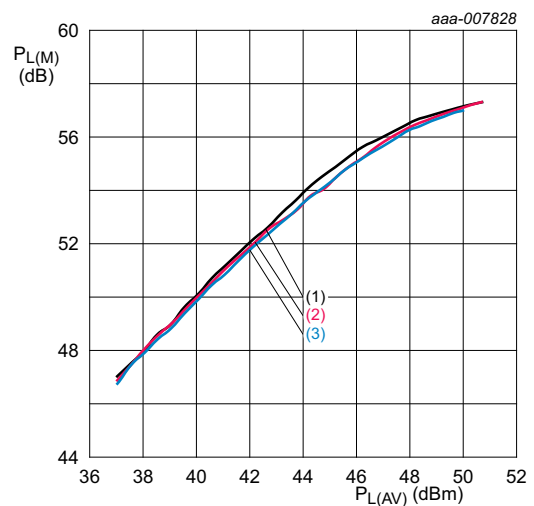
$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA}.$
 (1) $f = 1805\text{ MHz}$
 (2) $f = 1840\text{ MHz}$
 (3) $f = 1880\text{ MHz}$

Fig 11. Drain efficiency as a function of average output power; typical values



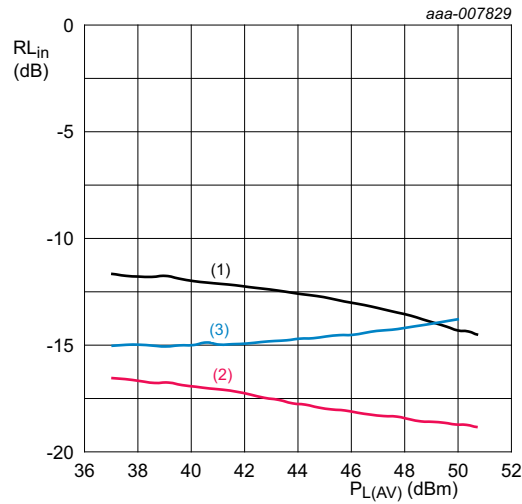
$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA}.$
 (1) $f = 1805\text{ MHz}$
 (2) $f = 1840\text{ MHz}$
 (3) $f = 1880\text{ MHz}$

Fig 12. Peak-to-average power ratio as a function of average output power; typical values



$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA}.$
 (1) $f = 1805\text{ MHz}$
 (2) $f = 1840\text{ MHz}$
 (3) $f = 1880\text{ MHz}$

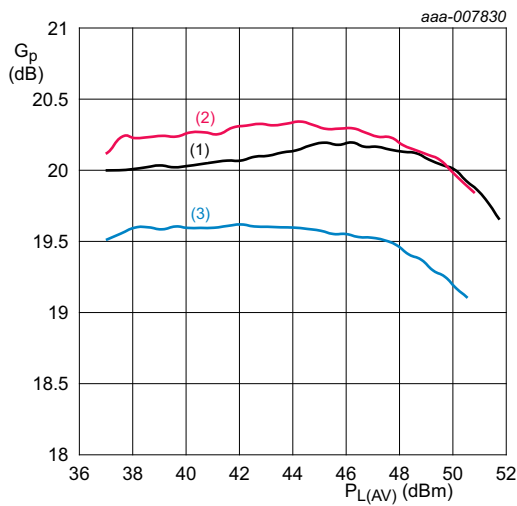
Fig 13. Peak output power as a function of average output power; typical values



$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA}$.
 (1) $f = 1805\text{ MHz}$
 (2) $f = 1840\text{ MHz}$
 (3) $f = 1880\text{ MHz}$

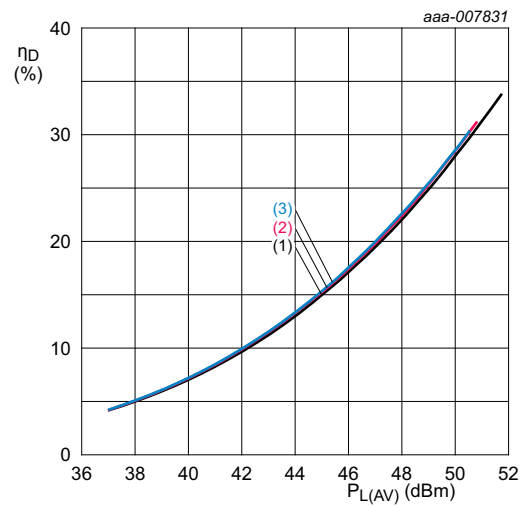
Fig 14. Input return loss as a function of average output power; typical values

7.5.4 1-Carrier W-CDMA



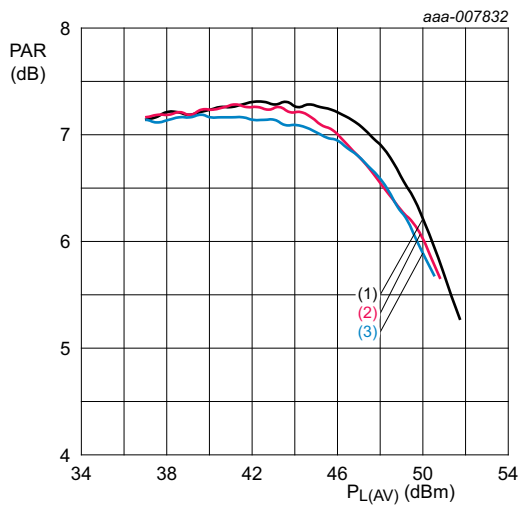
$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA}$.
 (1) $f = 1805\text{ MHz}$
 (2) $f = 1840\text{ MHz}$
 (3) $f = 1880\text{ MHz}$

Fig 15. Power gain as a function of average output power; typical values



$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA}$.
 (1) $f = 1805\text{ MHz}$
 (2) $f = 1840\text{ MHz}$
 (3) $f = 1880\text{ MHz}$

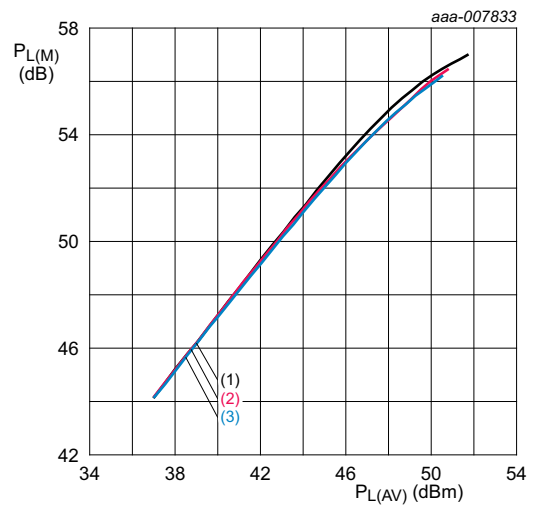
Fig 16. Drain efficiency as a function of average output power; typical values



$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA}$.

- (1) $f = 1805\text{ MHz}$
- (2) $f = 1840\text{ MHz}$
- (3) $f = 1880\text{ MHz}$

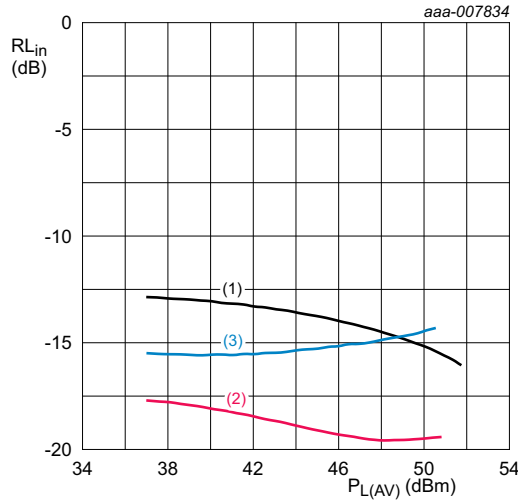
Fig 17. Peak-to-average power ratio as a function of average output power; typical values



$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA}$.

- (1) $f = 1805\text{ MHz}$
- (2) $f = 1840\text{ MHz}$
- (3) $f = 1880\text{ MHz}$

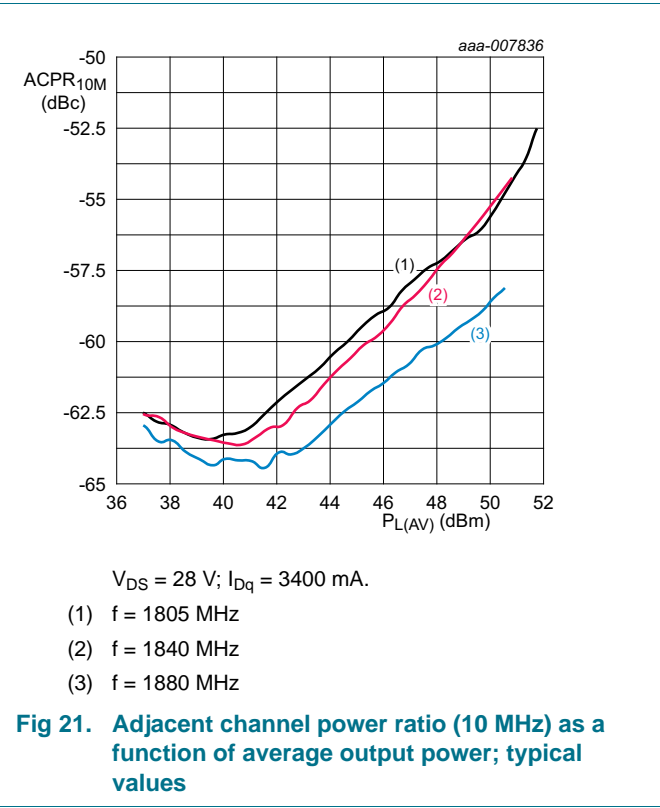
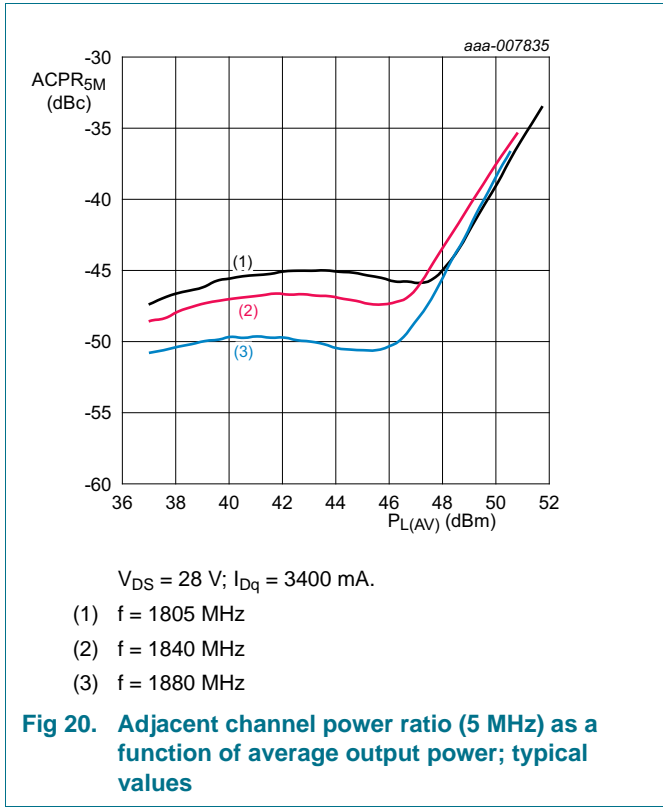
Fig 18. Peak output power as a function of average output power; typical values



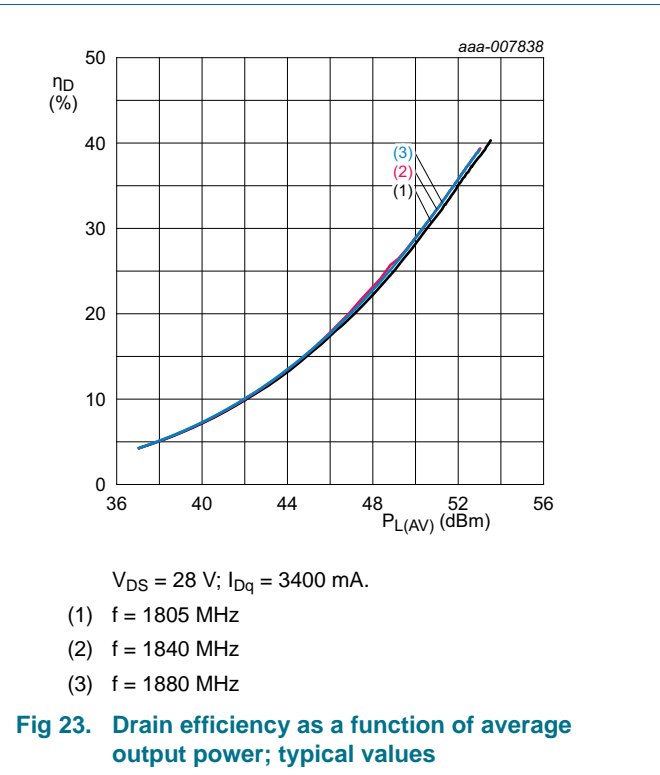
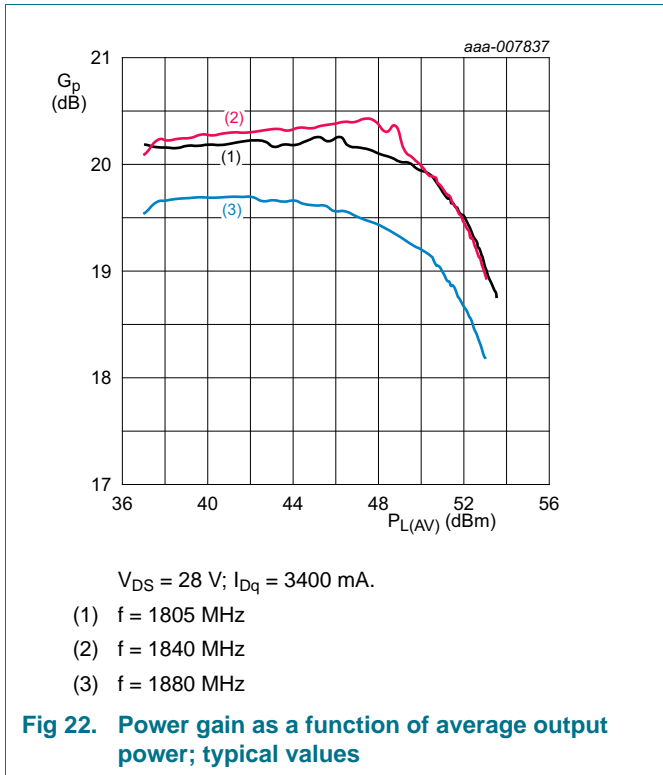
$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA}$.

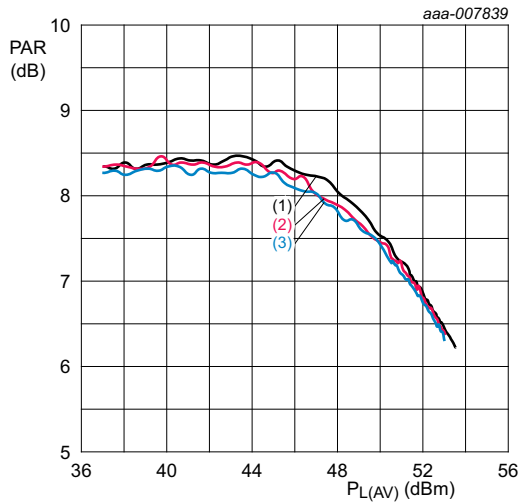
- (1) $f = 1805\text{ MHz}$
- (2) $f = 1840\text{ MHz}$
- (3) $f = 1880\text{ MHz}$

Fig 19. Input return loss as a function of average output power; typical values



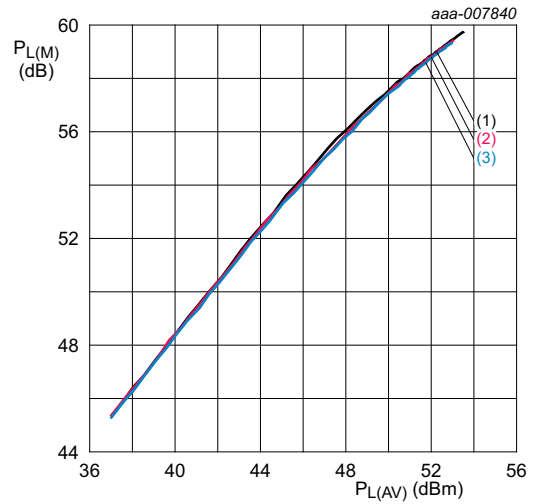
7.5.5 2-Carrier W-CDMA





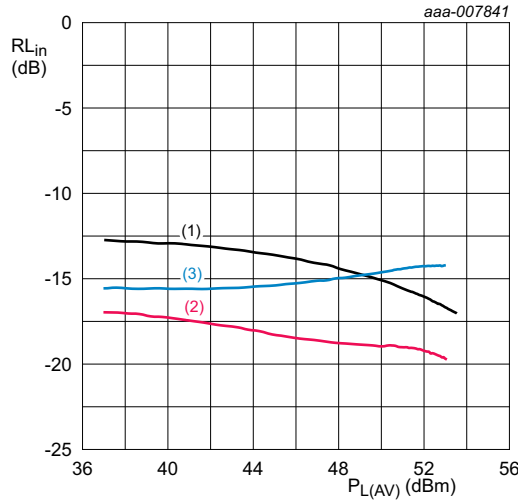
$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA}$.
 (1) $f = 1805\text{ MHz}$
 (2) $f = 1840\text{ MHz}$
 (3) $f = 1880\text{ MHz}$

Fig 24. Peak-to-average power ratio as a function of average output power; typical values



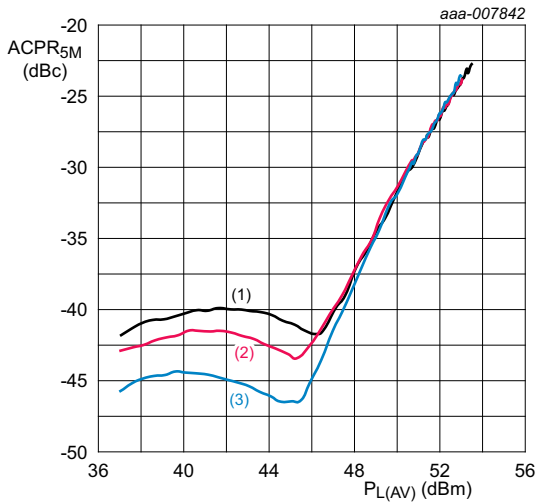
$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA}$.
 (1) $f = 1805\text{ MHz}$
 (2) $f = 1840\text{ MHz}$
 (3) $f = 1880\text{ MHz}$

Fig 25. Peak output power as a function of average output power; typical values



$V_{DS} = 28\text{ V}; I_{Dq} = 3400\text{ mA}$.
 (1) $f = 1805\text{ MHz}$
 (2) $f = 1840\text{ MHz}$
 (3) $f = 1880\text{ MHz}$

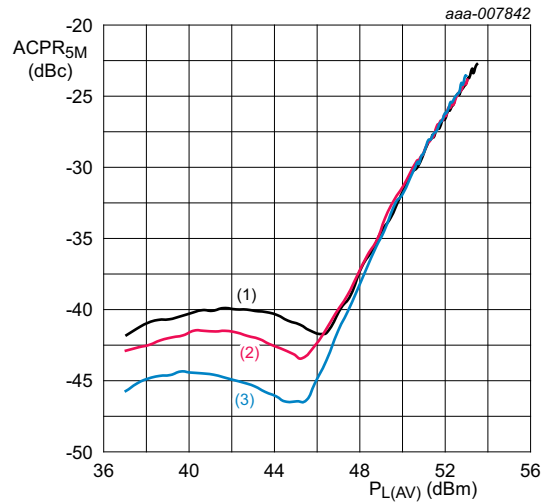
Fig 26. Input return loss as a function of average output power; typical values



$V_{DS} = 28\text{ V}; I_{DQ} = 3400\text{ mA}$.

- (1) $f = 1805\text{ MHz}$
- (2) $f = 1840\text{ MHz}$
- (3) $f = 1880\text{ MHz}$

Fig 27. Adjacent channel power ratio (5 MHz) as a function of average output power; typical values



$V_{DS} = 28\text{ V}; I_{DQ} = 3400\text{ mA}$.

- (1) $f = 1805\text{ MHz}$
- (2) $f = 1840\text{ MHz}$
- (3) $f = 1880\text{ MHz}$

Fig 28. Adjacent channel power ratio (10 MHz) as a function of average output power; typical values

8. Package outline

Earless flanged ceramic package; 8 leads

SOT1242B

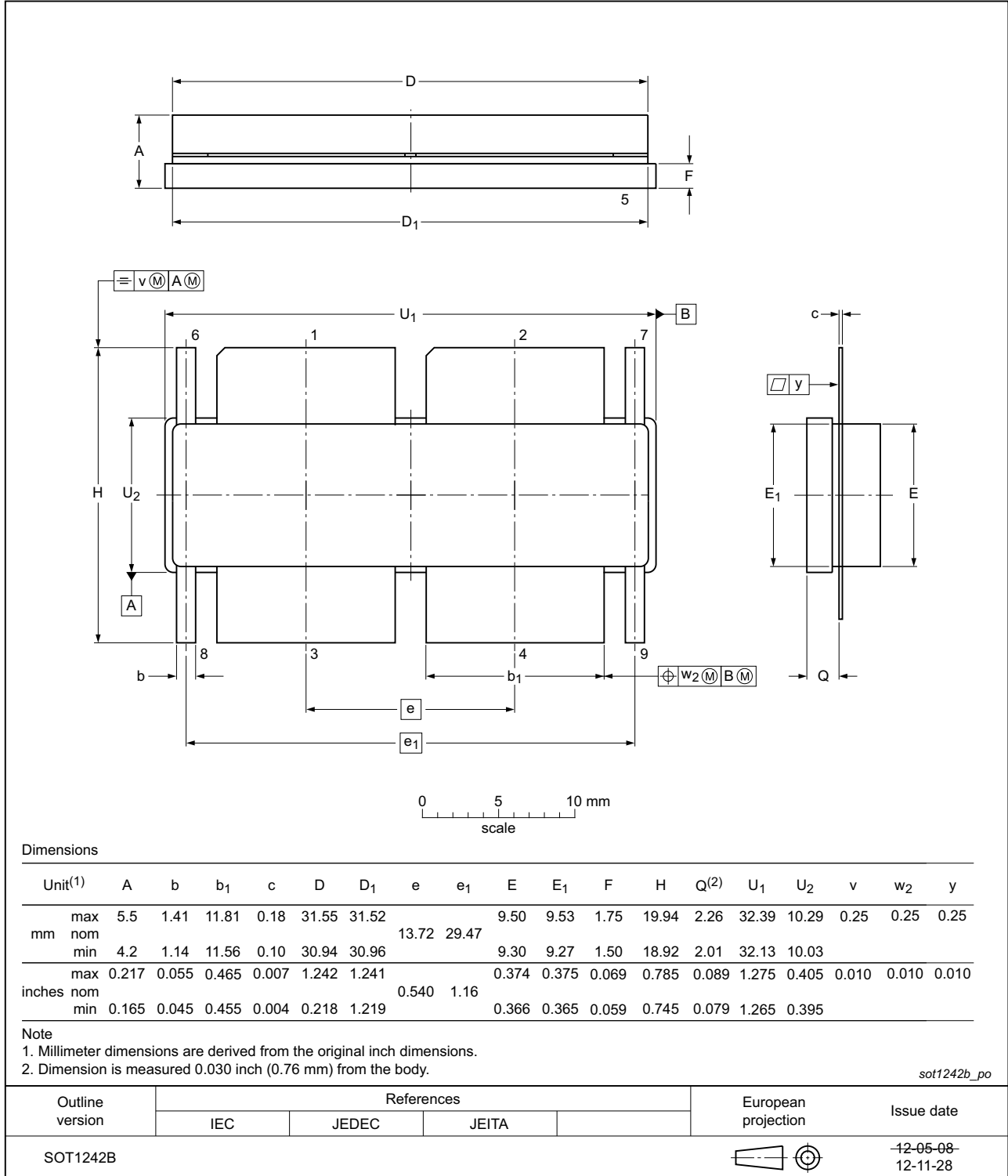


Fig 29. Package outline SOT1242B

Earless flanged ceramic package; 8 leads

SOT1242C

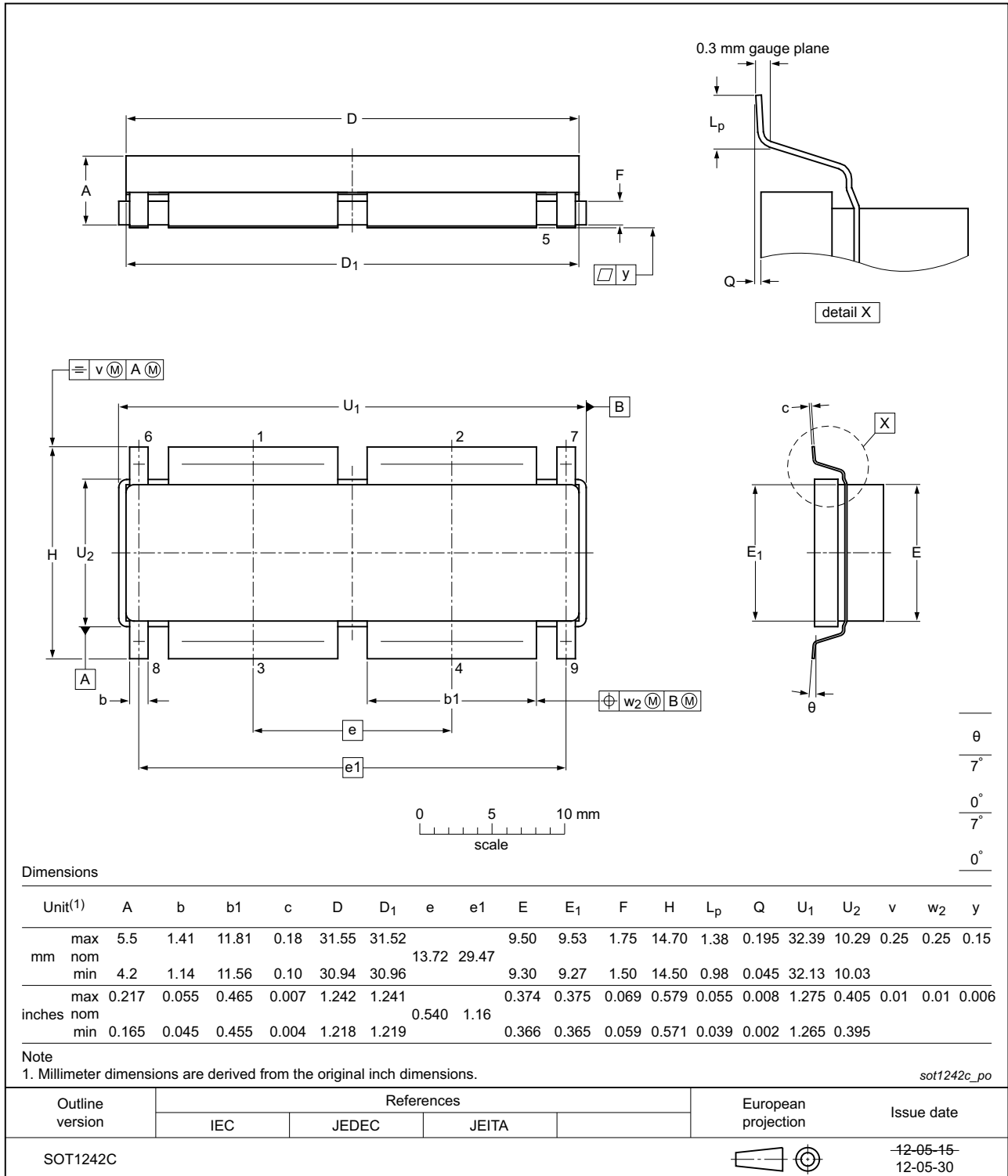


Fig 30. Package outline SOT1242C

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical Channel
ESD	ElectroStatic Discharge
IMD	InterModulation Distortion
IS-95	Interim Standard 95
LDMOS	Laterally Diffused Metal Oxide Semiconductor
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF8G20LS-400PV_LS-400PGV v.1	20130606	Preliminary data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

12.2 Definitions

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Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

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