Rochester Electronics

*Datasheet*

# PART NUMBER

# 54H73JC-ROCV

## Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All re-creations are done with the approval of the Original Component Manufacturer. (OCM)

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

## Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
    - Class Q Military
    - Class V Space Level

Qualified Suppliers List of Distributors (QSLD)

- Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

*The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OCM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.*

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Datasheet

# 54H73, 54L73

## *Dual J-K Flip-Flops with Clear*

The ‘H73, and ‘L73 contain two independent J-K flip-flops with individual J-K, clock, and direct clear inputs. J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low transition. For these devices the J and K inputs must be stable while the clock is high.

The SN54H73, SN54L73, and the SN54LS73A are characterized for operation over the full military temperature range of -55°C to 125°C.

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FOR REFERENCE ONLY

- **Package Options Include Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

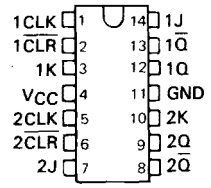
## description

The '73, 'H73, and 'L73 contain two independent J-K flip-flops with individual J-K, clock, and direct clear inputs. The '73, 'H73, and 'L73 are positive pulse-triggered flip-flops. J-K input is loaded into the master while the clock is high and transferred to the slave on the high-to-low transition. For these devices the J and K inputs must be stable while the clock is high.

The 'LS73A contain two independent negative-edge-triggered flip-flops. The J and K inputs must be stable one setup time prior to the high-to-low clock transition for predictable operation. When the clear is low, it overrides the clock and data inputs forcing the Q output low and the $\overline{Q}$ output high.

The SN5473, SN54H73, SN54L73, and the SN54LS73A are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7473, SN74H73, and the SN74LS73A are characterized for operation from 0°C to 70°C.

SN5473, SN54H73, SN54LS73A . . . J OR W PACKAGE
SN54L73 . . . J PACKAGE
SN7473, SN74H73 . . . J OR N PACKAGE
SN74LS73A . . . D, J OR N PACKAGE
(TOP VIEW)




'73, 'H73, 'L73
FUNCTION TABLE

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| $\overline{CLR}$ | CLK | J | K | Q | $\overline{Q}$ |
| L | X | X | X | L | H |
| H | ⎍ | L | L | $Q_0$ | $\overline{Q}_0$ |
| H | ⎍ | H | L | H | L |
| H | ⎍ | L | H | L | H |
| H | ⎍ | H | H | TOGGLE | |

'LS73A
FUNCTION TABLE

| INPUTS | | | | OUTPUTS | |
|---|---|---|---|---|---|
| $\overline{CLR}$ | CLK | J | K | Q | $\overline{Q}$ |
| L | X | X | X | L | H |
| H | ↓ | L | L | $Q_0$ | $\overline{Q}_0$ |
| H | ↓ | H | L | H | L |
| H | ↓ | L | H | L | H |
| H | ↓ | H | H | TOGGLE | |
| H | H | X | X | $Q_0$ | $Q_0$ |

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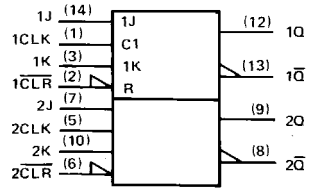
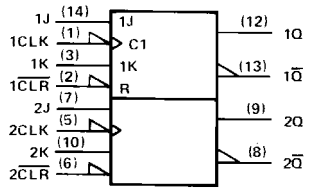
## logic symbols

'73, 'H73, 'L73



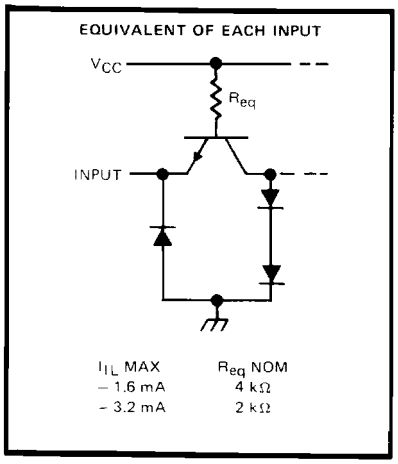

'LS73A

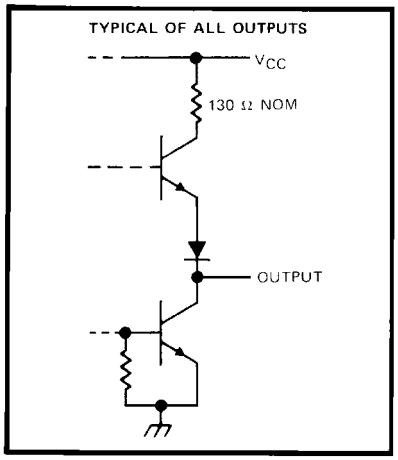



Pin numbers shown on logic notation are for D, J or N packages.

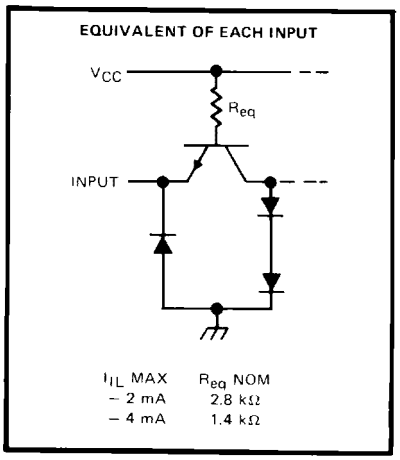
## schematics of inputs and outputs

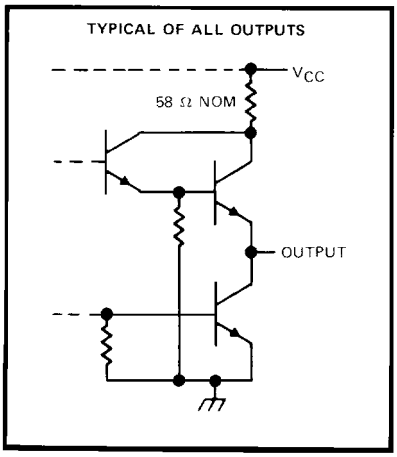
'73




'H73





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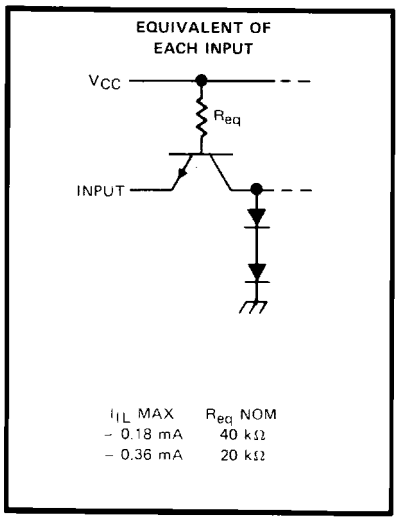
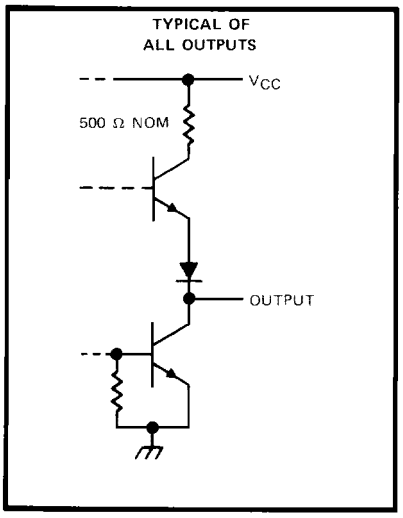
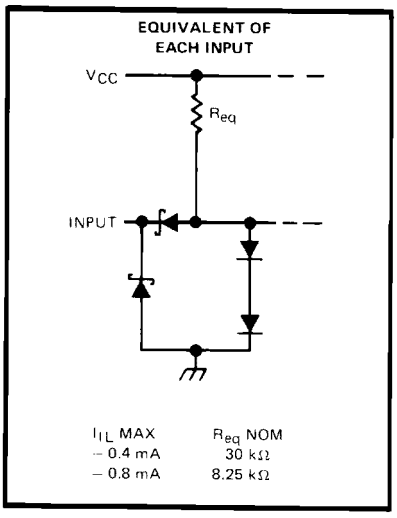
schematics of inputs and outputs (continued)

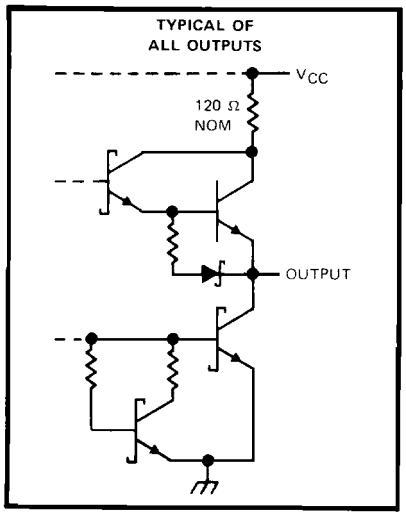
'L73



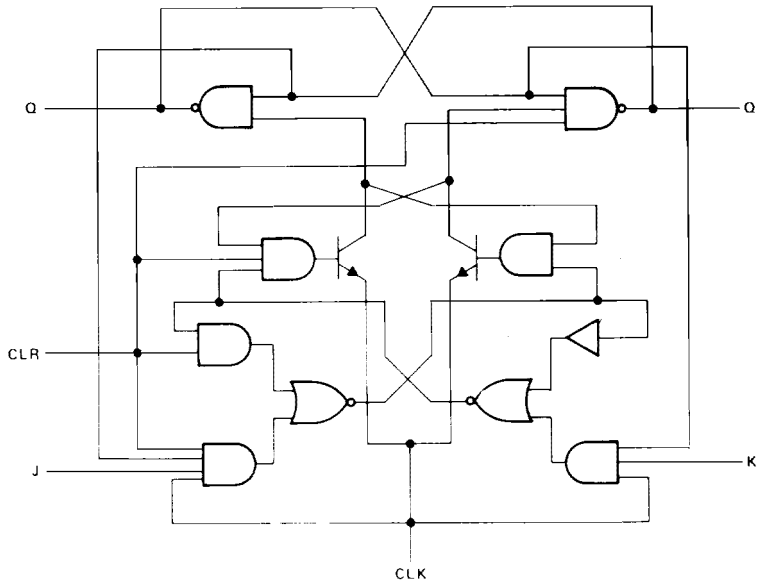

'LS73A



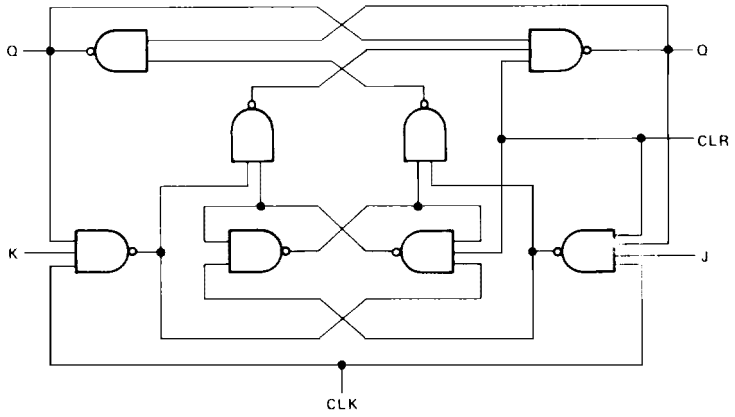



logic diagrams

'73




'H73





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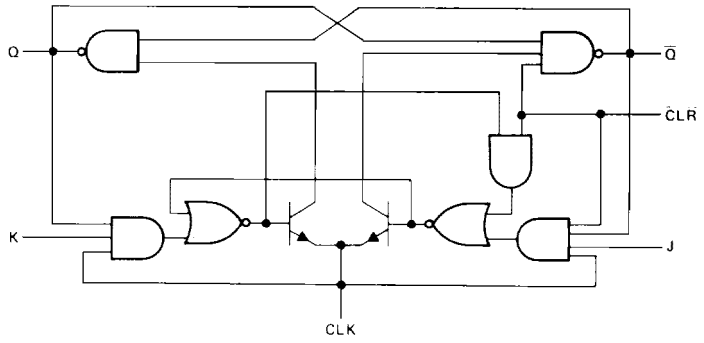
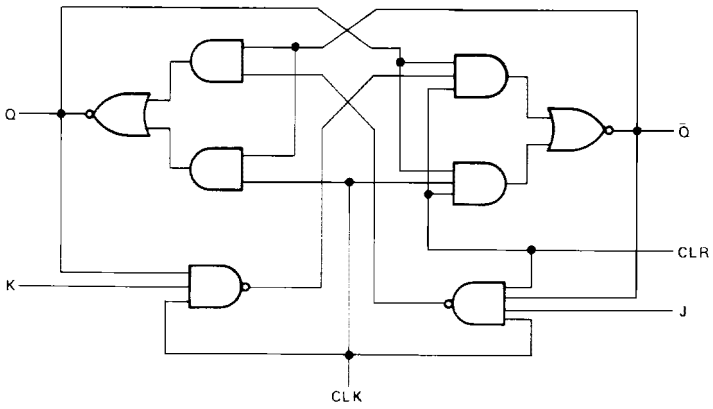
**logic diagrams (continued)**

'L73




'LS73A




**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)**

Supply voltage, $V_{CC}$ (see Note 1) . . . . . 7 V
Input voltage: '73, 'H73, 'L73 . . . . . 5.5 V
'LS73A . . . . . 7 V
Operating free-air temperature range: SN54' . . . . . −55°C to 125°C
SN74' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

## recommended operating conditions

| | | | SN5473 | | | SN7473 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | −0.4 | | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | | | | 16 | | | 16 | mA |
| $t_w$ | Pulse duration | CLK high | 20 | | | 20 | | | ns |
| | | CLK low | 47 | | | 47 | | | |
| | | $\overline{CLR}$ low | 25 | | | 25 | | | |
| $t_{su}$ | Input setup time before CLK↑ | | 0 | | | 0 | | | ns |
| $t_h$ | Input hold time data after CLK↓ | | 0 | | | 0 | | | ns |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | | SN5473 | | | SN7473 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | | $V_{CC}$ = MIN, | $I_I$ = −12 mA | | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | | $V_{CC}$ = MIN, $I_{OH}$ = −0.4 mA | $V_{IH}$ = 2 V, | $V_{IL}$ = 0.8 V, | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| $V_{OL}$ | | $V_{CC}$ = MIN, $I_{OL}$ = 16 mA | $V_{IH}$ = 2 V, | $V_{IL}$ = 0.8 V, | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| $I_I$ | | $V_{CC}$ = MAX, | $V_I$ = 5.5 V | | | | 1 | | | 1 | mA |
| $I_{IH}$ | J or K | $V_{CC}$ = MAX, | $V_I$ = 2.4 V | | | | 40 | | | 40 | μA |
| | $\overline{CLR}$ or CLK | | | | | | 80 | | | 80 | |
| $I_{IL}$ | J or K | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | | −1.6 | | | −1.6 | mA |
| | $\overline{CLR}$ | | | | | | −3.2 | | | −3.2 | |
| | CLK | | | | | | −3.2 | | | −3.2 | |
| $I_{OS}$§ | | $V_{CC}$ = MAX | | | −20 | | −57 | −18 | | −57 | mA |
| $I_{CC}$ | | $V_{CC}$ = MAX, | See Note 2 | | | 10 | 20 | | 10 | 20 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 2: With all outputs open, $I_{CC}$ is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C (see note 3)

| PARAMETER¶ | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{max}$ | | | $R_L$ = 400 Ω, $C_L$ = 15 pF | 15 | 20 | | MHz |
| $t_{PLH}$ | $\overline{CLR}$ | $\overline{Q}$ | | | 16 | 25 | ns |
| $t_{PHL}$ | | Q | | | 25 | 40 | ns |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | | | 16 | 25 | ns |
| $t_{PHL}$ | | | | | 25 | 40 | ns |

¶ $f_{max}$ = maximum clock frequency; $t_{PLH}$ = propagation delay time, low-to-high-level output; $t_{PHL}$ = propagation delay time, high-to-low-level output.
NOTE 3: See General Information Section for load circuits and voltage waveforms.





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## recommended operating conditions

| | | | SN54H73 | | | SN74H73 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.8 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | −0.5 | | | −0.5 | mA |
| $I_{OL}$ | Low-level output current | | | | 20 | | | 20 | mA |
| $t_w$ | Pulse duration | CLK high | 12 | | | 12 | | | ns |
| | | CLK low | 28 | | | 28 | | | |
| | | $\overline{CLR}$ low | 16 | | | 16 | | | |
| $t_{su}$ | Input setup time before CLK↑ | High-level data | 0 | | | 0 | | | ns |
| | | Low-level data | 0 | | | 0 | | | |
| $t_h$ | Input hold time, data after CLK↓ | | 0 | | | 0 | | | ns |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | | SN54H73 | | | SN74H73 | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | | $V_{CC}$ = MIN, | $I_I$ = −8 mA | | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | | $V_{CC}$ = MIN, $I_{OH}$ = −0.5 mA | $V_{IH}$ = 2 V, | $V_{IL}$ = 0.8 V | 2.4 | 3.4 | | 2.4 | 3.4 | | V |
| $V_{OL}$ | | $V_{CC}$ = MIN, $I_{OL}$ = 20 mA | $V_{IH}$ = 2 V, | $V_{IL}$ = 0.8 V, | | 0.2 | 0.4 | | 0.2 | 0.4 | V |
| $I_I$ | | $V_{CC}$ = MAX, | $V_I$ = 5.5 V | | | | 1 | | | 1 | mA |
| $I_{IH}$ | J, K, or CLK | $V_{CC}$ = MAX, | $V_I$ = 2.4 V | | | | 50 | | | 50 | μA |
| | $\overline{CLR}$ | | | | | | 100 | | | 100 | |
| $I_{IL}$ | J, K, or CLK | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | | −2 | | | −2 | mA |
| | $\overline{CLR}$ | | | | | | −4 | | | −4 | |
| $I_{OS}$§ | | $V_{CC}$ = MAX | | | −40 | | −100 | −40 | | −100 | mA |
| $I_{CC}$ | | $V_{CC}$ = MAX, | See Note 2 | | | 16 | 25 | | 16 | 25 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: With all outputs open, $I_{CC}$ is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C (see note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{max}$ | | | $R_L$ = 280 Ω, $C_L$ = 25 pF | 25 | 30 | | MHz |
| $t_{PLH}$ | $\overline{CLR}$ | $\overline{Q}$ | | | 6 | 13 | ns |
| $t_{PHL}$ | | Q | | | 12 | 24 | ns |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | | | 14 | 21 | ns |
| $t_{PHL}$ | | | | | 22 | 27 | ns |

NOTE 3: See General Information Section for load circuits and voltage waveforms

## recommended operating conditions

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | Clock input | | | 0.6 | V |
| | | All other inputs | | | 0.7 | |
| $I_{OH}$ | High-level output current | | | | −0.1 | mA |
| $I_{OL}$ | Low-level output current | | | | 2 | mA |
| $t_w$ | Pulse duration | CLK high or low | 200 | | | ns |
| | | $\overline{CLR}$ low | 100 | | | |
| $t_{su}$ | Setup time before CLK ↑ | | 0 | | | ns |
| $t_h$ | Hold time-data after CLK ↓ | | 0 | | | ns |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwire noted)

| PARAMETER | | TEST CONDITIONS† | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{OH}$ | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = MAX, $I_{OH}$ = −0.1 mA | 2.4 | 3.3 | | V |
| $V_{OL}$ | | $V_{CC}$ = MIN, $V_{IH}$ = 2 V, $V_{IL}$ = MAX, $I_{OL}$ = 2 mA | | 0.15 | 0.3 | V |
| $I_I$ | J or K | $V_{CC}$ = MAX, $V_I$ = 5.5 V | | | 0.1 | mA |
| | $\overline{CLR}$ or CLK | | | | 0.2 | |
| $I_{IH}$ | J or K | $V_{CC}$ = MAX, $V_I$ = 2.4 V | | | 10 | μA |
| | $\overline{CLR}$ | | | | 20 | |
| | CLK | | | | −200 | |
| $I_{IL}$ | J or K | $V_{CC}$ = MAX, $V_I$ = 0.3 V | | | −0.18 | mA |
| | $\overline{CLR}$ or CLK | | | | −0.36 | |
| $I_{OS}$ | | $V_{CC}$ = MAX | −3 | | −15 | mA |
| $I_{CC}$ | | $V_{CC}$ = MAX, See Note 2 | | 0.76 | 1.44 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
NOTE 2: With all outputs open, $I_{CC}$ is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C (see note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{max}$ | | | $R_L$ = 4 kΩ, $C_L$ = 50 pF | 2.5 | 3 | | MHz |
| $t_{PLH}$ | $\overline{CLR}$ | Q or $\overline{Q}$ | | | 35 | 75 | ns |
| $t_{PHL}$ | $\overline{CLR}$ (CLK high) | $\overline{Q}$ or Q | | | 60 | 150 | ns |
| | $\overline{CLR}$ (CLK low) | | | | | 200 | |
| $t_{PLH}$ | CLK | Q or $\overline{Q}$ | | 10 | 35 | 75 | ns |
| $t_{PHL}$ | | | | 10 | 60 | 150 | ns |

NOTE 3: See General Information Section for load circuits and voltage waveforms.





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## recommended operating conditions

| | | | SN54LS73A | | | SN74LS73A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | NOM | MAX | MIN | NOM | MAX | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5 | 5.5 | 4.75 | 5 | 5.25 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.7 | | | 0.8 | V |
| $I_{OH}$ | High-level output current | | | | −0.4 | | | −0.4 | mA |
| $I_{OL}$ | Low-level output current | | | | 4 | | | 8 | mA |
| $f_{clock}$ | Clock frequency | | 0 | | 30 | 0 | | 30 | MHz |
| $t_w$ | Pulse duration | CLK high | 20 | | | 20 | | | ns |
| | | $\overline{CLR}$ low | 25 | | | 20 | | | |
| $t_{su}$ | Set up time-before CLK↓ | data high or low | 20 | | | 20 | | | ns |
| | | $\overline{CLR}$ inactive | 20 | | | 20 | | | |
| $t_h$ | Hold time-data after CLK↓ | | 0 | | | 0 | | | ns |
| $T_A$ | Operating free-air temperature | | −55 | | 125 | 0 | | 70 | °C |

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS† | | SN54LS73A | | | SN74LS73A | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP‡ | MAX | MIN | TYP‡ | MAX | |
| $V_{IK}$ | | $V_{CC}$ = MIN, | $I_I$ = −18 mA | | | −1.5 | | | −1.5 | V |
| $V_{OH}$ | | $V_{CC}$ = MIN, $I_{OH}$ = −0.4 mA | $V_{IH}$ = 2 V, $V_{IL}$ = MAX, | 2.5 | 3.4 | | 2.7 | 3.4 | | V |
| $V_{OL}$ | | $V_{CC}$ = MIN, $I_{OL}$ = 4 mA | $V_{IL}$ = MAX, $V_{IH}$ = 2 V, | | 0.25 | 0.4 | | 0.25 | 0.4 | V |
| | | $V_{CC}$ = MIN, $I_{OL}$ = 8 mA | $V_{IL}$ = MAX, $V_{IH}$ = 2 V, | | | | | 0.35 | 0.5 | |
| $I_I$ | J or K | $V_{CC}$ = MAX, | $V_I$ = 7 V | | | 0.1 | | | 0.1 | mA |
| | $\overline{CLR}$ | | | | | 0.3 | | | 0.3 | |
| | CLK | | | | | 0.4 | | | 0.4 | |
| $I_{IH}$ | J or K | $V_{CC}$ = MAX, | $V_I$ = 2.7 V | | | 20 | | | 20 | μA |
| | $\overline{CLR}$ | | | | | 60 | | | 60 | |
| | CLK | | | | | 80 | | | 80 | |
| $I_{IL}$ | J or K | $V_{CC}$ = MAX, | $V_I$ = 0.4 V | | | −0.4 | | | −0.4 | mA |
| | $\overline{CLR}$ or CLK | | | | | −0.8 | | | −0.8 | |
| $I_{OS}$§ | | $V_{CC}$ = MAX, | See Note 4 | −20 | | −100 | −20 | | −100 | mA |
| $I_{CC}$ | | $V_{CC}$ = MAX, | See Note 2 | | 4 | 6 | | 4 | 6 | mA |

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at $V_{CC}$ = 5 V, $T_A$ = 25°C.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.
NOTE 2: With all outputs open, $I_{CC}$ is measured with the Q and $\overline{Q}$ outputs high in turn. At the time of measurement, the clock input is grounded.
NOTE 4: For certain devices where state commutation can be caused by shorting an output to ground, an equivalent test may be performed with $V_O$ = 2.25 V and 2.125 V for the 54 family and the 74 family, respectively, with the minimum and maximum limits reduced to one half of their stated values.

## switching characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C (see note 3)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $f_{max}$ | $\overline{CLR}$ or CLK | Q or $\overline{Q}$ | $R_L$ = 2 kΩ, $C_L$ = 15 pF | 30 | 45 | | MHz |
| $t_{PLH}$ | | | | | 15 | 20 | ns |
| $t_{PHL}$ | | | | | 15 | 20 | ns |

NOTE 3: See General Information Section for load circuits and voltage waveforms.