

18V Low Current Consumption 300mA CMOS Voltage Regulator

LR6302 Series

■ INTRODUCTION

The LR6302 series are a group of positive voltage regulators manufactured by CMOS technologies with low power consumption and low dropout voltage, which provide large output currents even when the difference of the input-output voltage is small. The LR6302 series can deliver 300mA output current and allow an input voltage as high as 18V. The series are very suitable for the battery-powered equipments, such as RF applications and other systems requiring a quiet voltage source.

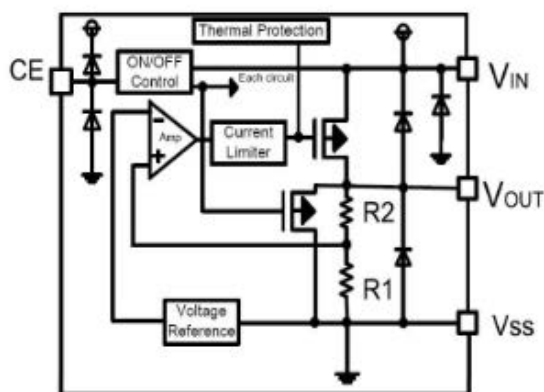
■ APPLICATIONS

- Cordless Phones
- Radio control systems
- Laptop, Palmtops and PDAs
- Single-lens reflex DSC
- PC peripherals with memory

■ FEATURES

- Low Quiescent Current: 2 μ A
- Operating Voltage Range: 2.5V~18V
- Output Current: 300mA
- Low Dropout Voltage:
160mV@100mA($V_{OUT}=3.3V$)
- Output Voltage: 1.2~ 5.0V
- High Accuracy: $\pm 2\%/ \pm 1\%$ (Typ.)
- High Power Supply Rejection Ratio:
65dB@1kHz
- Low Output Noise:
27x V_{OUT} μ V_{RMS} (10Hz~100kHz)
- Excellent Line and Load Transient Response
- Built-in Current Limiter, Short-Circuit Protection
- Over-Temperature Protection
For LR6302A and LR6302B only
- Wireless Communication Equipments
- Portable Audio Video Equipments
- Car Navigation Systems
- LAN Cards
- Ultra Low Power Microcontroller

■ BLOCK DIAGRAM



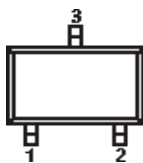
■ ORDER INFORMATION

LR6302①②③④⑤

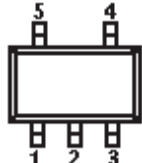
DESIGNATOR	SYMBOL	DESCRIPTION
①	A	Without EN
	B	With Shutdown Function
	D	Without OTP
②③	Integer	Output Voltage e.g. 1.8V=②:1, ③:8
④	M/ MC/ MY	Package:SOT-23-3
	M/MF/MR	Package:SOT-23-5
	P/PT/PL	Package:SOT-89-3
	F	Package:DFN1x1-4
	FT	Package:DFN2020-6
	SL	Package:SOT223
⑤	-	2% Accuracy
	1	1% Accuracy

PIN CONFIGURATION

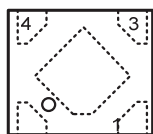
SOT-23-3



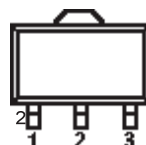
SOT-23-5



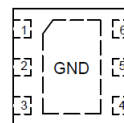
DFN1×1-4



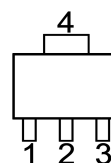
SOT-89-3



DFN2020-6



SOT-223



LR6302A

PIN NUMBER						PIN NAME	FUNCTION
SOT-23-3			SOT-89-3				
M	MC	MY	P	PT	PL		
1	3	3	1	2	2	V _{SS}	Ground
2	2	1	3	1	3	V _{OUT}	Output
3	1	2	2	3	1	V _{IN}	Power input

PIN NUMBER			PIN NAME	FUNCTION
SOT-23-5		SOT-223		
MF	MR	SL		
1	2	3	V _{IN}	Power Input
2	1	1	V _{SS}	Ground
3/4	4/5	-	NC	No Connection
5	3	2/4	V _{OUT}	Output

LR6302B

PIN NUMBER	SYMBOL	FUNCTION
SOT-23-5		
M		
1	V _{IN}	Power Input Pin
2	V _{SS}	Ground
3	CE	Chip Enable Pin
4	NC	No Connection
5	V _{OUT}	Output Pin

PIN NUMBER	SYMBOL	FUNCTION
DFN1×1-4		
F		
1	V _{OUT}	Output Pin
2	V _{SS}	Ground
3	CE	Chip Enable Pin
4	V _{IN}	Power Input Pin

PIN NUMBER	SYMBOL	FUNCTION
DFN2020-6		
F		
1	V _{OUT}	Output Pin
2	NC	No Connection
3	GND	Ground
4	CE	Chip Enable Pin
5	NC	No Connection
6	V _{IN}	Power Input Pin

■ ABSOLUTE MAXIMUM RATINGS⁽¹⁾

 (Unless otherwise specified, $T_A=25^{\circ}\text{C}$)

PARAMETER		SYMBOL	RATINGS	UNITS
Input Voltage ⁽²⁾		V_{IN}	-0.3~24	V
Output Voltage ⁽²⁾		V_{OUT}	-0.3~10	V
CE Pin Voltage		V_{CE}	-0.3~24	V
Output Current		I_{OUT}	600	mA
Thermal Resistance	SOT-23-5 ⁽³⁾	R_{thja}	200	$^{\circ}\text{C}/\text{W}$
		R_{thjc}	50	$^{\circ}\text{C}/\text{W}$
Power Dissipation	SOT-23-3	P_D	0.3	W
	SOT-23-5		0.3	W
	SOT-89-3		0.5	W
	DFN1X1-4		0.4	W
	DFN2X2-6		0.5	W
Operating Junction Temperature Range ⁽⁴⁾		T_j	-40~125	$^{\circ}\text{C}$
Storage Temperature		T_{stg}	-40~125	$^{\circ}\text{C}$
Lead Temperature(Soldering, 10 sec)		T_{solder}	260	$^{\circ}\text{C}$
ESD rating ⁽⁵⁾		Human Body Model -(HBM)	2000	V
		Machine Model- (MM)	250	V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are with respect to network ground terminal.

(3) Thermal resistance test board size: 30.0mm×25.0mm×1.6mm (FR4); Copper foil thickness: 35um.

Recommended soldering pad. R0JC test point is at the center position directly above the plastic encapsulation.

(4) The LR6302A includes over temperature protection that is intended to protect the device during momentary overload. Junction temperature will exceed 125 $^{\circ}\text{C}$ when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

(5) ESD testing is performed according to the respective AEC-Q100 standard.

The human body model is a 100 pF capacitor discharged through a 1.5k Ω resistor into each pin. The machine model is a 200pF capacitor discharged directly into each pin.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN.	NOM.	MAX.	UNITS
Supply voltage at V_{IN}	2.5		18	V
Operating junction temperature range, T_j	-40		125	$^{\circ}\text{C}$
Operating free air temperature range, T_A	-40		85	$^{\circ}\text{C}$

■ ELECTRICAL CHARACTERISTICS

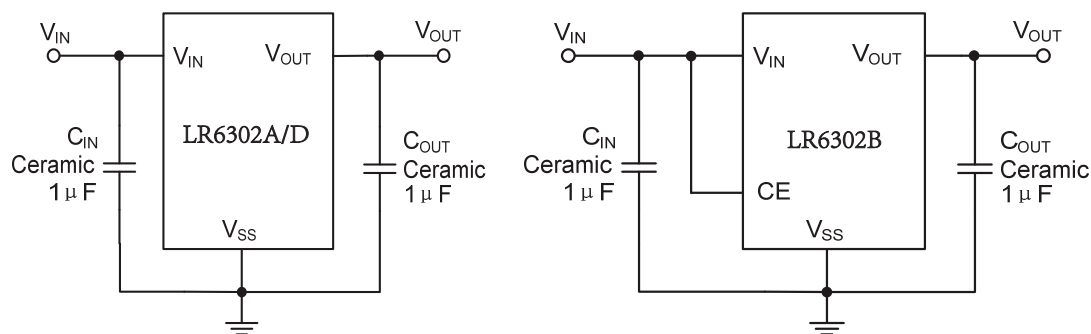
LR6302 Series
($V_{IN}=V_{OUT}+1V$, $C_{IN}=C_{OUT}=1\mu F$, $T_A=25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP. ⁽⁵⁾	MAX.	UNITS
Input Voltage	V_{IN}		2.5	—	18	V
Output Voltage Range	V_{OUT}		1.2	—	5	V
DC Output Accuracy		$I_{OUT}=1mA$	-2	—	2	%
			-1	—	1	%
Dropout Voltage	$V_{dif}^{(6)}$	$I_{OUT}=100mA, V_{OUT}=3.3V$	—	160	—	mV
Supply Current	I_{SS}	$I_{OUT}=0A$	—	2	5	μA
Line Regulation	$\frac{\Delta V_{OUT}}{V_{OUT} \times \Delta V_{IN}}$	$I_{OUT}=10mA$ $V_{OUT}+1V \leq V_{IN} \leq 18V$	—	0.01	0.3	%/V
Load Regulation	ΔV_{OUT}	$V_{IN}=V_{OUT}+1V$, $1mA \leq I_{OUT} \leq 100mA$	—	10	—	mV
Temperature Coefficient	$\frac{\Delta V_{OUT}}{V_{OUT} \times \Delta T_A}$	$I_{OUT}=10mA$, $-40^\circ C < T_A < 125^\circ C$		50		ppm
Output Current Limit	I_{LIM}	$V_{OUT}=0.5 \times V_{OUT(Normal)}$, $V_{IN}=5V$	350	500	-	mA
Short Current	I_{SHORT}	$V_{OUT}=V_{SS}$	—	25	—	mA
Power Supply Rejection Ratio	PSRR	$I_{OUT}=50mA$	100Hz	80		dB
			1kHz	65	—	
			10kHz	50	—	
			100kHz	45	—	
Output Noise Voltage	V_{ON}	BW=10Hz to 100kHz	—	$27 \times V_{OUT}$	—	μV_{RMS}
Thermal Shutdown Temperature	T_{SD}	—	—	150	—	$^\circ C$
Thermal Shutdown Hysteresis	ΔT_{SD}	—	—	20	—	$^\circ C$
Standby Current	I_{STBY}	$CE = V_{SS}$			0.2	μA
CE "High" Voltage	$V_{CE"H"}$		1.5		V_{IN}	V
CE "Low" Voltage	$V_{CE"L"}$				0.3	V
C_{OUT} Auto-Discharge Resistance	$R_{DISCHRG}$	$V_{IN}=5V, V_{OUT}=3.0V$, $V_{CE}=V_{SS}$		150		Ω

 (5) Typical numbers are at $25^\circ C$ and represent the most likely norm.

 (6) V_{dif} : The Difference Of Output Voltage And Input Voltage When Input Voltage Is Decreased Gradually Till Output Voltage Equals To 98% Of V_{OUT} (E).

■ TYPICAL APPLICATION CIRCUIT



■ APPLICATION INFORMATION

Selection of Input/ Output Capacitors

In general, all the capacitors need to be low leakage. Any leakage the capacitors have will reduce efficiency, increase the quiescent current.

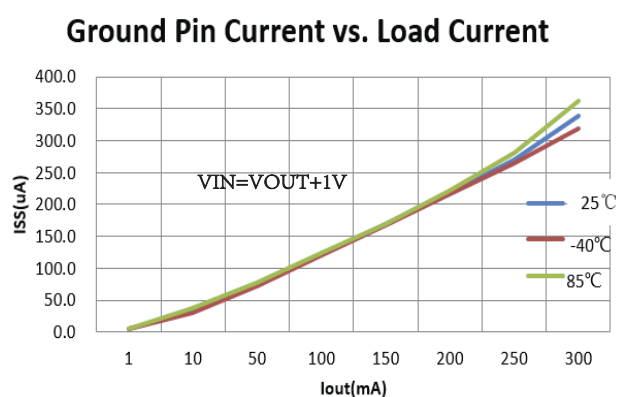
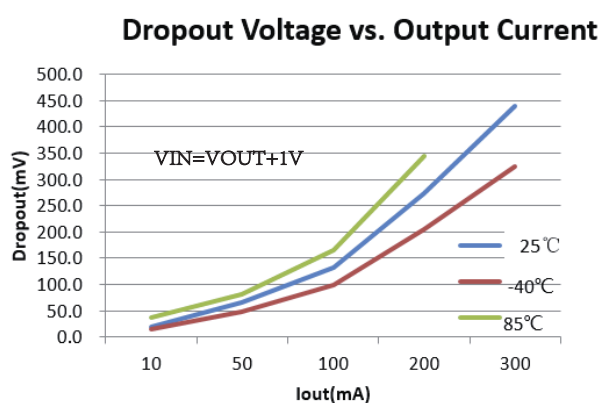
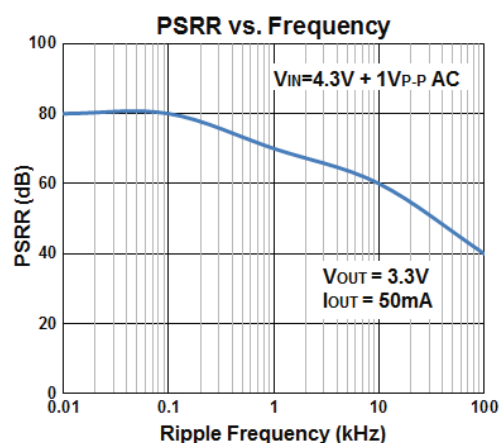
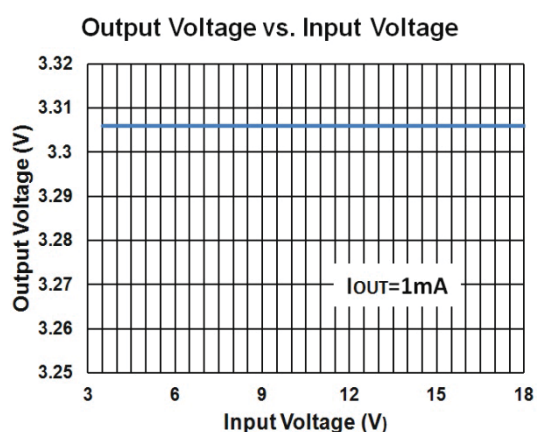
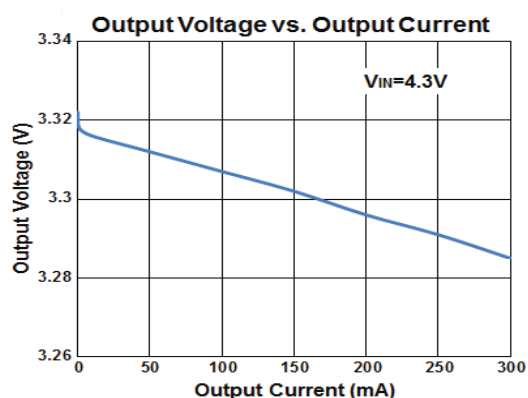
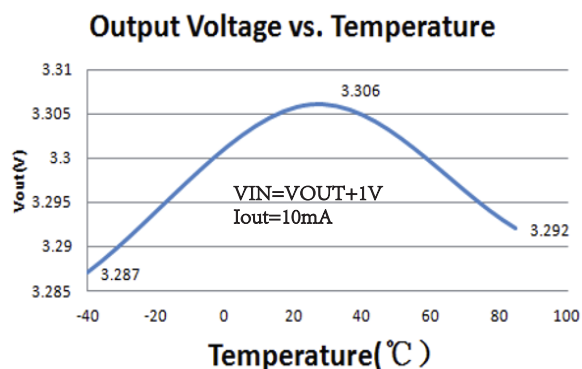
A recent trend in the design of portable devices has been to use ceramic capacitors to filter DC-DC converter inputs. Ceramic capacitors are often chosen because of their small size, low equivalent series resistance (ESR) and high RMS current capability. Also, recently, designers have been looking to ceramic capacitors due to shortages of tantalum capacitors.

Unfortunately, using ceramic capacitors for input filtering can cause problems. Applying a voltage step to a ceramic capacitor causes a large current surge that stores energy in the inductances of the power leads. A large voltage spike is created when the stored energy is transferred from these inductances into the ceramic capacitor. These voltage spikes can easily be twice the amplitude of the input voltage step. (See “Ceramic Input Capacitors Can Cause Overvoltage Transients”——Linear Technology application note 88, March 2001)

Many types of capacitors can be used for input bypassing, however, caution must be exercised when using multilayer ceramic capacitors (MLCC). Because of the self-resonant and high Q characteristics of some types of ceramic capacitors, high voltage transients can be generated under some start-up conditions, such as connecting the LDO input to a live power source. Adding a 3Ω resistor in series with an X5R ceramic capacitor will minimize start-up voltage transients.

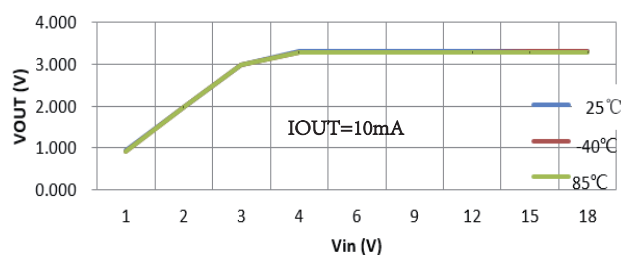
The LDO also requires an output capacitor for loop stability. Connect a $1\mu F$ tantalum capacitor from OUT to GND close to the pins. For improved transient response, this output capacitor may be ceramic.

■ TYPICAL PERFORMANCE CHARACTERISTICS

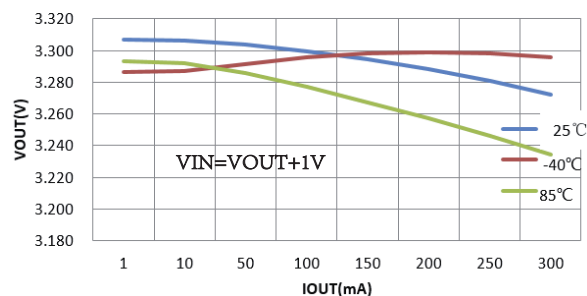


■ TYPICAL PERFORMANCE CHARACTERISTICS (continued)

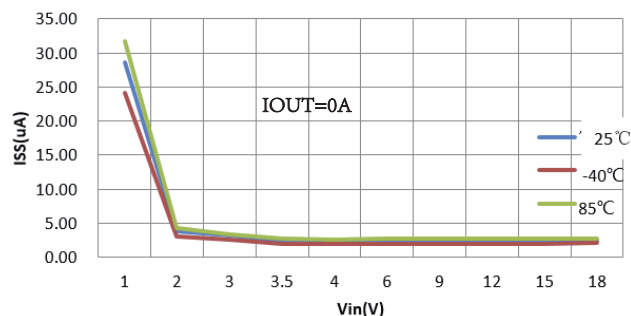
Line Regulation



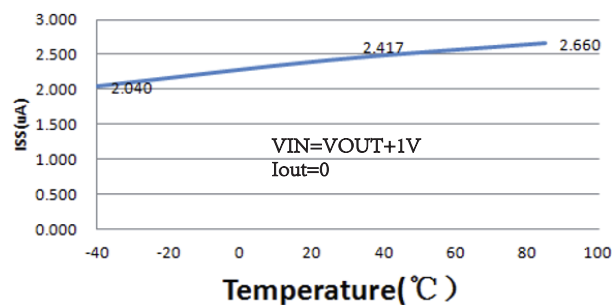
Load Regulation



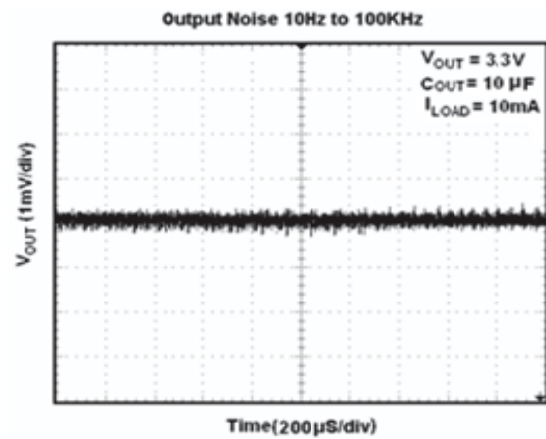
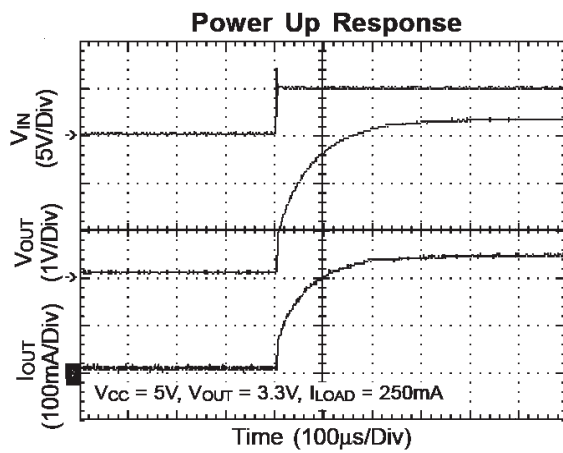
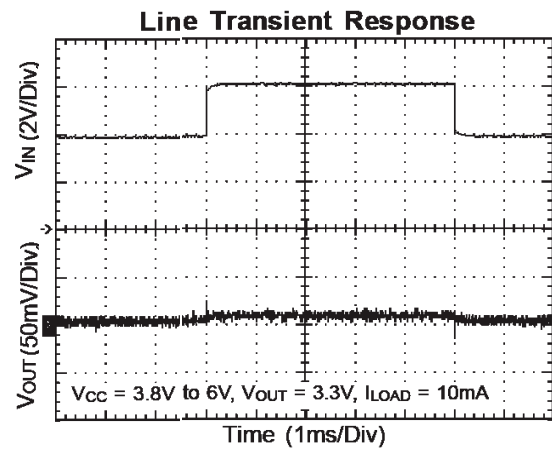
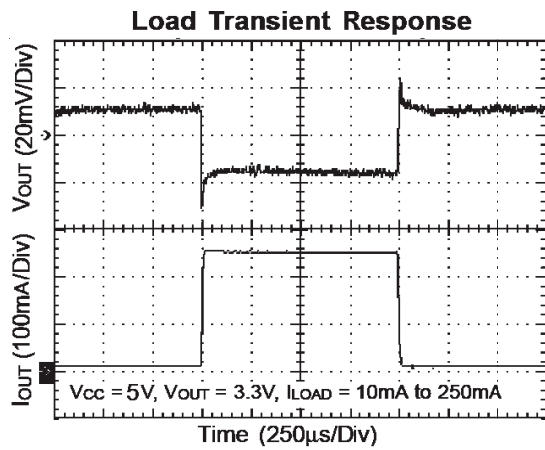
Ground Pin Current vs. Input Voltage



Ground Current vs. Temperature

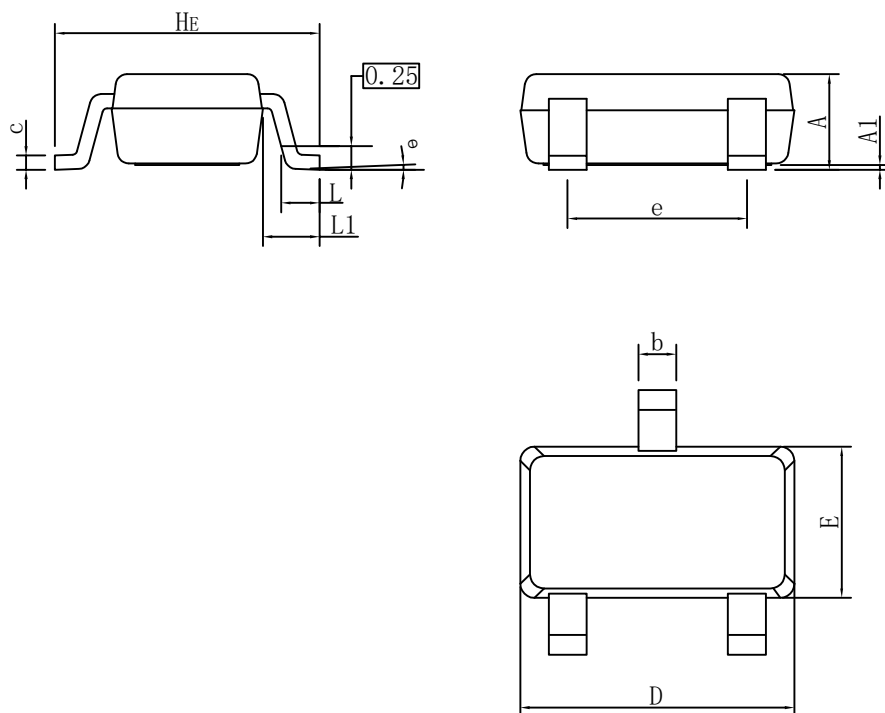


■ TYPICAL PERFORMANCE CHARACTERISTICS (continued)



■ PACKAGING INFORMATION

• SOT-23-3 PACKAGE OUTLINE DIMENSIONS

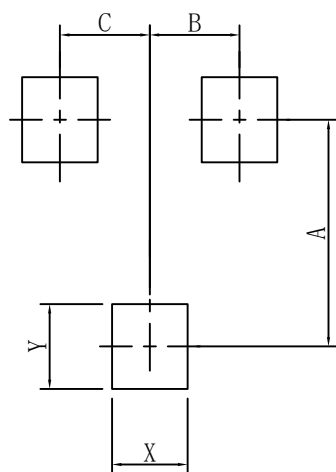


SOT23LC			
DIM	MIN	NOR	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.30	0.40	0.50
c	0.10	0.17	0.20
D	2.80	2.90	3.00
E	1.50	1.60	1.70
e	1.80	1.90	2.00
L	0.20	0.40	0.60
L1	0.60REF		
HE	2.60	2.80	3.00
θ	0°	-	10°
All Dimensions in mm			

GENERAL NOTES

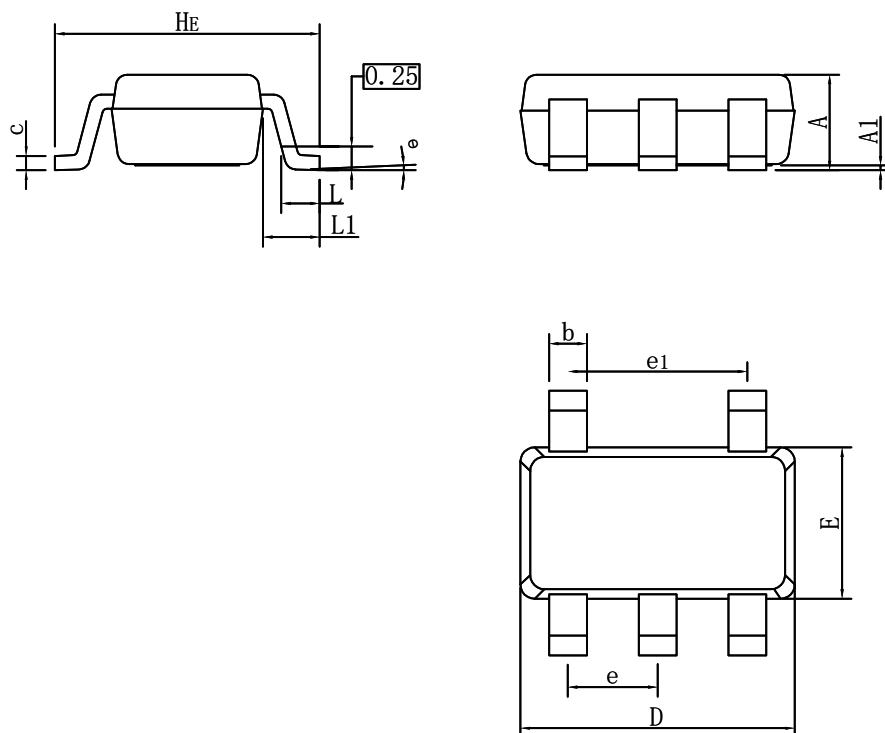
- 1.Top package surface finish $Ra0.4\pm0.2\mu m$
- 2.Bottom package surface finish $Ra0.7\pm0.2\mu m$
- 3.Side package surface finish $Ra0.4\pm0.2\mu m$

• RECOMMENDED PAD LAYOUT



DIM	(mm)
X	0.80
Y	0.90
A	2.40
B	0.95
C	0.95

• SOT-23-5 PACKAGE OUTLINE DIMENSIONS

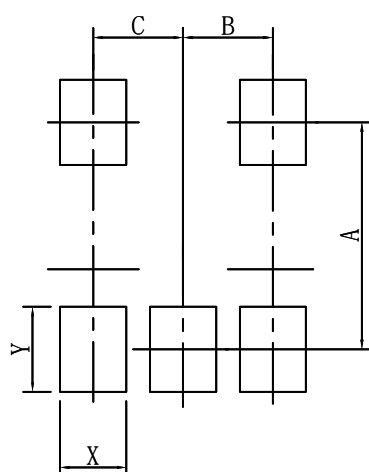


SOT25			
DIM	MIN	NOR	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.30	0.40	0.50
c	0.10	0.17	0.20
D	2.80	2.90	3.00
E	1.50	1.60	1.70
e	0.85	0.95	1.05
e1	1.80	1.90	2.00
L	0.20	0.40	0.60
L1	0.60REF		
HE	2.60	2.80	3.00
θ	0°	-	10°

GENERAL NOTES

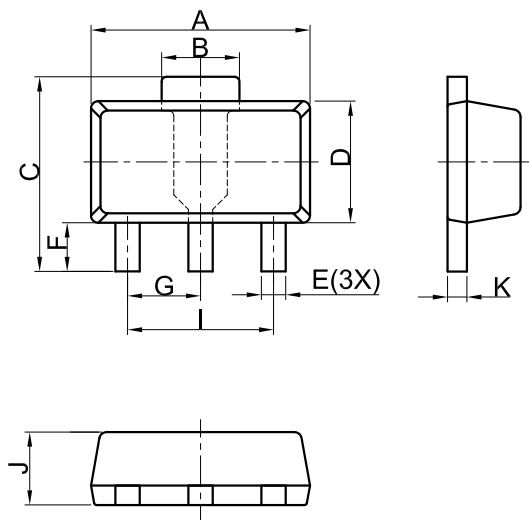
- 1.Top package surface finish $Ra0.4\pm0.2\mu m$
- 2.Bottom package surface finish $Ra0.7\pm0.2\mu m$
- 3.Side package surface finish $Ra0.4\pm0.2\mu m$

• RECOMMENDED PAD LAYOUT



SOT25	
DIM	(mm)
X	0.70
Y	0.90
A	2.40
B	0.95
C	0.95

• **SOT-89-3 PACKAGE OUTLINE DIMENSIONS**

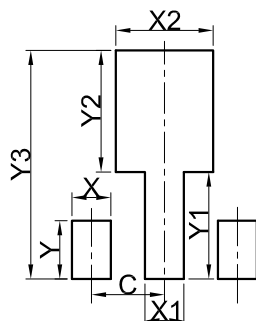


SOT89			
DIM	MIN	NOR	MAX
A	4.30	4.50	4.70
B	1.40	1.60	1.80
C	3.90	4.00	4.25
D	2.30	2.50	2.70
E	0.40	0.50	0.58
F	0.90	1.00	1.20
G	1.50 BSC		
I	3.00 BSC		
J	1.40	1.50	1.60
K	0.34	0.40	0.50
All Dimensions in mm			

GENERAL NOTES

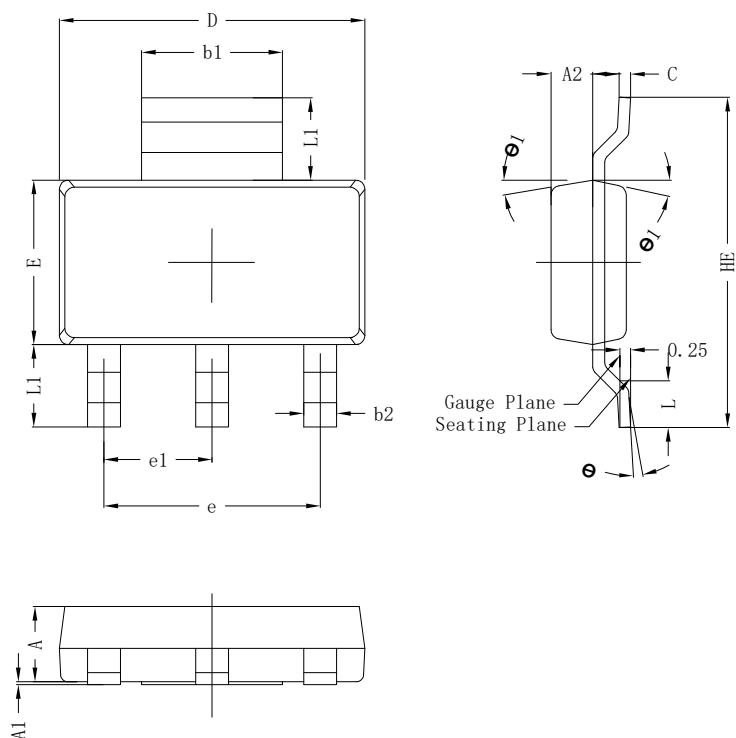
1. Top package surface finish $Ra0.4\pm0.2\mu m$
2. Bottom package surface finish $Ra0.7\pm0.2\mu m$
3. Side package surface finish $Ra0.4\pm0.2\mu m$
4. Protrusion or Gate Burrs shall not exceed 0.10mm per side.

• **RECOMMENDED PAD LAYOUT**



SOT89-3	
DIM	(mm)
X	0.80
Y	1.20
X1	0.80
Y1	2.20
X2	2.00
Y2	2.50
C	1.50
Y3	4.70

• SOT-223 PACKAGE OUTLINE DIMENSIONS

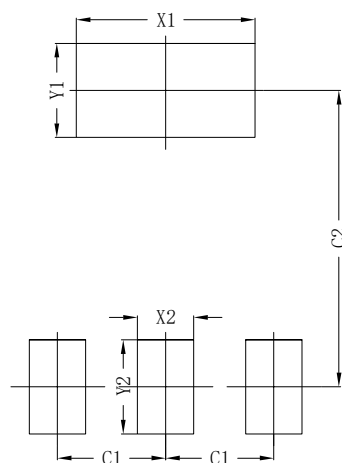


SOT223			
DIM	MIN	NOR	MAX
A	1.50	1.60	1.70
A1	0.00	0.05	0.10
A2	0.80	0.90	1.00
b1	2.90	3.02	3.10
b2	0.60	0.72	0.80
c	0.20	0.27	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	4.60BSC		
e1	2.30BSC		
HE	6.80	7.00	7.20
L	0.80	1.00	1.20
L1	1.75(REF)		
θ	0°~8°		
θ 1	8°	10°	12°
All Dimensions in mm			

GENERAL NOTES

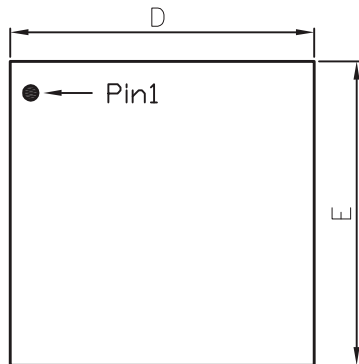
1. Top package surface finish $Ra0.4 \pm 0.2\mu m$
2. Bottom package surface finish $Ra0.7 \pm 0.2\mu m$
3. Side package surface finish $Ra0.4 \pm 0.2\mu m$
4. Protrusion or Gate Burrs shall not exceed 0.10mm per side.

• RECOMMENDED PAD LAYOUT

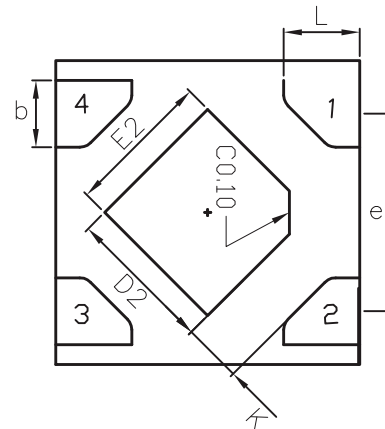


SOT223	
DIM	(mm)
X1	3.80
Y1	2.00
X2	1.20
Y2	2.00
C1	2.30
C2	6.30

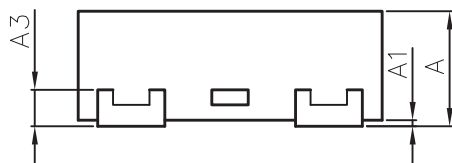
• DFN1×1-4 PACKAGE OUTLINE DIMENSIONS



TOP VIEW



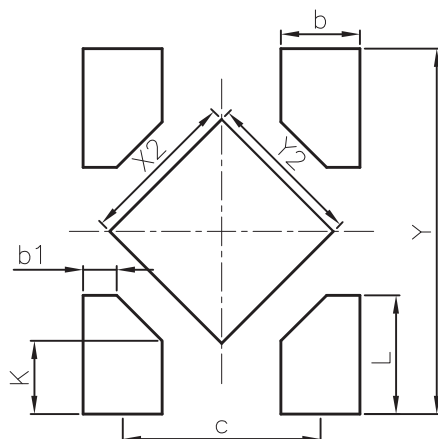
BOTTOM VIEW



SIDE VIEW

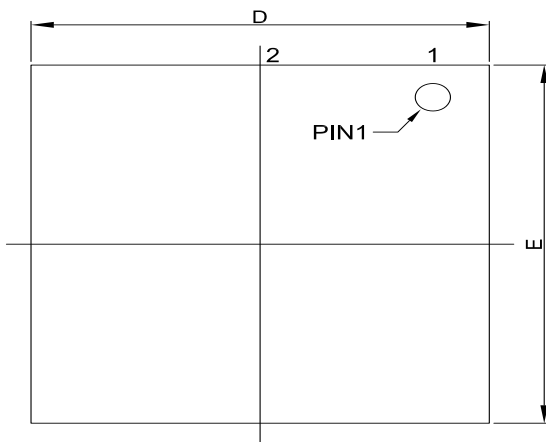
DFN1010			
DIM	MIN	NOR	MAX
A	0.34	0.37	0.40
A1	0.01	0.02	0.05
b	0.17	0.22	0.25
L	0.20	0.25	0.30
D	0.95	1.00	1.05
E	0.95	1.00	1.05
D2	0.43	0.48	0.53
E2	0.43	0.48	0.53
e	0.65		
A3	0.127REF.		
K	0.15	-	-
All Dimensions in mm			

• RECOMMENDED PAD LAYOUT

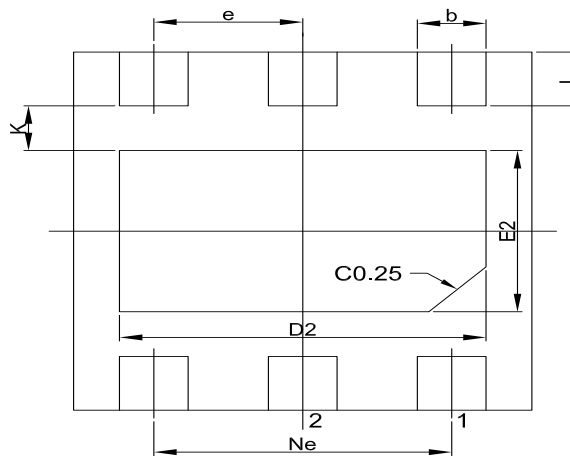


DFN1010	
DIM	(mm)
X2	0.52
Y2	0.52
L	0.39
Y	1.20
K	0.24
b	0.26
c	0.65
b1	0.11

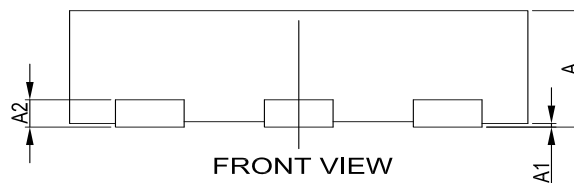
• **DFN2020-6 PACKAGE OUTLINE DIMENSIONS**



TOP VIEW



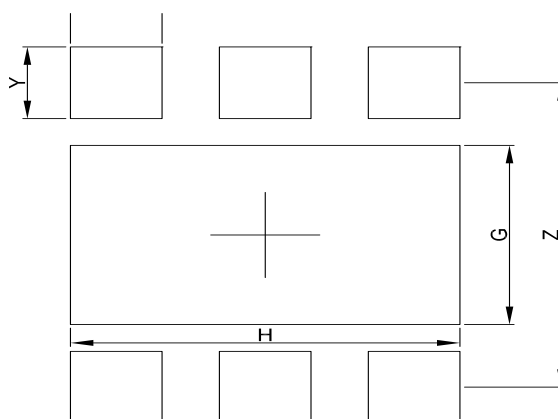
BOTTOM VIEW



FRONT VIEW

DIM	MILLIMETER		
	MIN	NOM	MAX
A	0.60	0.65	0.70
A ₁	---	0.02	0.05
A ₂	0.152 REF		
b	0.25	0.30	0.35
D	1.95	2.00	2.05
D2	1.50	1.60	1.70
Ne	1.30 BSC		
e	0.65 BSC		
E	1.95	2.00	2.05
E2	0.85	0.90	0.95
L	0.25	0.30	0.35
K	0.20	0.25	0.30

• **RECOMMENDED PAD LAYOUT**



Dimensions	(mm)
G	1.00
H	1.70
J	0.65
X	0.40
Y	0.40
Z	1.70

ORDERING INFORMATION

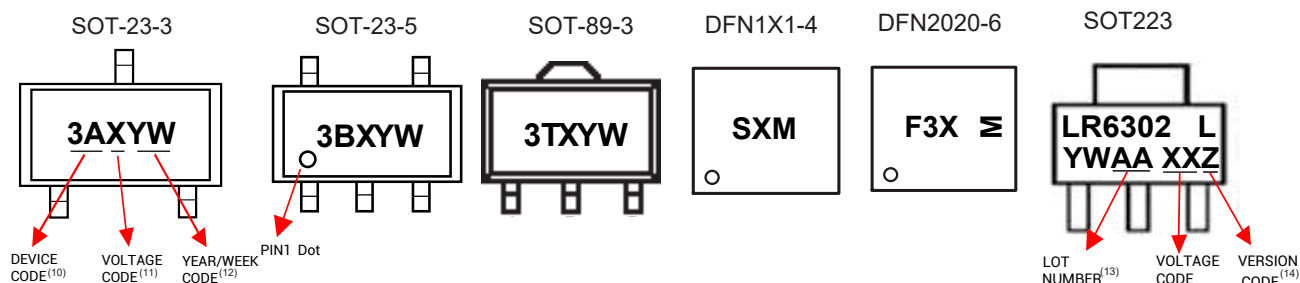
Device ⁽⁷⁾	Package	Output Voltage ⁽⁸⁾	Marking ⁽⁹⁾	Shipping
LR6302AxxM	SOT-23-3	1.2V~5.0 V	3AX	3K/Reel
LR6302AxxM1	SOT-23-3	1.2V~5.0V	3AX	3K/Reel
LR6302AxxMC	SOT-23-3	1.2V~5.0 V	3CX	3K/Reel
LR6302AxxMY	SOT-23-5	1.2V~5.0 V	3YX	3K/Reel
LR6302AxxMF	SOT-23-5	1.2V~5.0 V	3FX	3K/Reel
LR6302AxxMR	SOT-23-5	1.2V~5.0 V	3RX	3K/Reel
LR6302BxxM	SOT-23-5	1.2V~5.0 V	3BX	3K/Reel
LR6302BxxM1	SOT-23-5	1.2V~5.0 V	3BX	3K/Reel
LR6302AxxP	SOT-89-3	1.2V~5.0 V	3DX	5K/Reel
LR6302AxxPT	SOT-89-3	1.2V~5.0 V	3TX	5K/Reel
LR6302AxxPL	SOT-89-3	1.2V~5.0 V	3LX	5K/Reel
LR6302BxxF	DFN1X1-4	1.2V~5.0 V	SX	12K/Reel
LR6302BxxFT	DFN2020-6	1.2V~5.0 V	F3X	5K/Reel
LR6302AxxSL	SOT223	1.2V~5.0 V	LR6302 L	4K/Reel

(7) The "xx" in part number represents output voltage, eg "18" = 1.8V, "50" = 5.0V.

(8) Output voltage varies from 1.2V to 5.0V, 0.1V an interval.

(9) There are additional marking, which relates to the date code. For detailed information, please refer to MARKING INFORMATION APPENDIX below.

MARKING INFORMATION APPENDIX



(10) The first two letters in the Marking represent DEVICE CODE. For DFN1X1-4 package, DEVICE CODE has only one letter.

(11) The following letter "X" in the Marking changes along with the output voltage, as the chart shows below.

Voltage(V)	1.2	1.5	1.8	2.5	2.5 (1%)	2.7	2.8	3.0	3.0 (1%)	3.3	3.3 (1%)	3.6	4.0	5.0	5.0 (1%)
Symbol	E	F	G	H	X	I	J	K	B	L	Q	M	N	P	m

(12) The last two letters in the Marking represent YEAR/WEEK CODE.

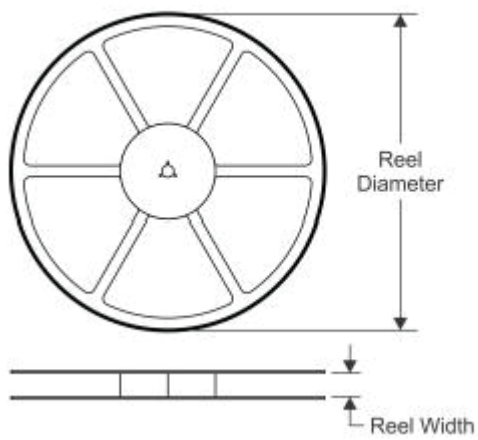
For DFN1X1-4 package, YEAR/WEEK CODE has only one letter.

For DFN2020-6 package, YEAR/WEEK CODE has only one letter and needs to be rotated by 90 degrees counterclockwise

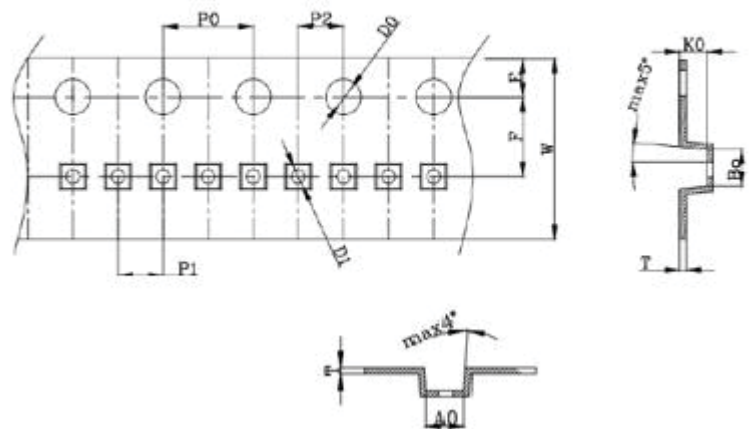
(13) (14) The LOT NUMBER and VERSION CODE are only used for internal production control of the factory.

■ TAPE AND REEL INFORMATION

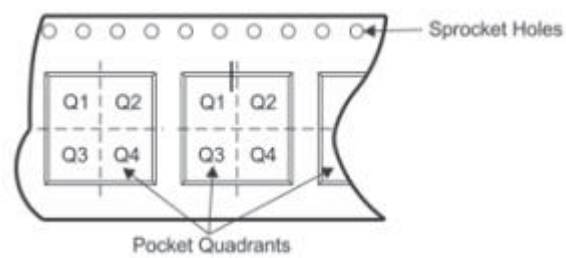
REEL DIMENSIONS



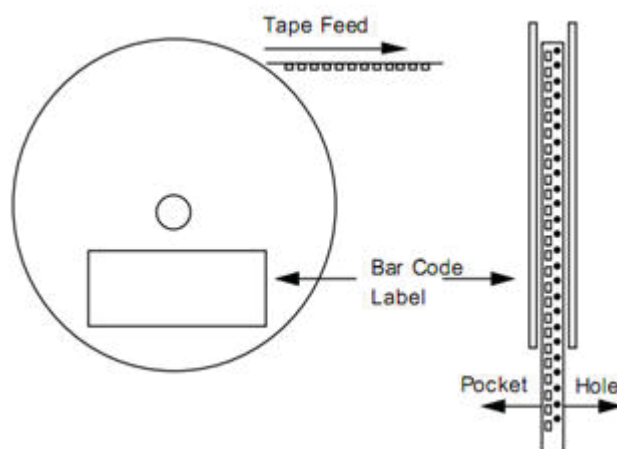
TAPE DIMENSIONS



PIN ORIENTATION



ROLLING ORIENTATION



Device	Package	Reel Diameter (mm)	Reel width (mm)	P0 (mm)	P1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	W (mm)	PIN1
LR6302AxxM	SOT-23-3	178±1	9.6±1.2	4.00±0.1	4.00±0.1	3.1±0.1	3.28±0.1	1.32±0.1	8.0±0.1	NA
LR6302AxxMC	SOT-23-3	178±1	9.6±1.2	4.00±0.1	4.00±0.1	3.1±0.1	3.28±0.1	1.32±0.1	8.0±0.1	NA
LR6302AxxMY	SOT-23-3	178±1	9.6±1.2	4.00±0.1	4.00±0.1	3.1±0.1	3.28±0.1	1.32±0.1	8.0±0.1	NA
LR6302AxxMF	SOT-23-5	178±1	9.6±1.2	4.00±0.1	4.00±0.1	3.25±0.05	3.15±0.05	1.5±0.05	8.0±0.1	NA
LR6302AxxMR	SOT-23-5	178±1	9.6±1.2	4.00±0.1	4.00±0.1	3.25±0.05	3.15±0.05	1.5±0.05	8.0±0.1	Q3
LR6302BxxM	SOT-23-5	178±1	9.6±1.2	4.00±0.1	4.00±0.1	3.25±0.05	3.15±0.05	1.5±0.05	8.0±0.1	Q3
LR6302AxxP	SOT-89-3	330±1.5	13.0 ⁺¹ _{-0.5}	4.00±0.1	8.00±0.1	4.75±0.1	4.2±0.1	1.75±0.1	12.0 ^{+0.3} _{-0.1}	NA
LR6302AxxPT	SOT-89-3	330±1.5	13.0 ⁺¹ _{-0.5}	4.00±0.1	8.00±0.1	4.75±0.1	4.2±0.1	1.75±0.1	12.0 ^{+0.3} _{-0.1}	NA
LR6302AxxPL	SOT-89-3	330±1.5	13.0 ⁺¹ _{-0.5}	4.00±0.1	8.00±0.1	4.75±0.1	4.2±0.1	1.75±0.1	12.0 ^{+0.3} _{-0.1}	NA
LR6302BxxF	DFN1X1-4	178±1	9.6±1.2	4.00±0.1	2.00±0.05	1.16±0.05	1.16±0.05	0.5±0.05	8.0±0.1	Q3
LR6302BxxFT	DFN2X2-6	178±1	9.6±1.2						8.0±0.1	Q1

■ REVISION HISTORY

Version	Description	Update by	Update Date
2.3	Update the the SOT89 device reel information from 1k/reel to 5k/reel. Add the SOT223 device information.	Chen S	2024-08-27
2.4	Add SOT25 thermal resistance and test conditions.	Chen S	2024-11-06
2.5	Update DFN1010-4 packing quantity from 10K/reel to 12K/reel. Update DFN2020-6 packing quantity from 4K/reel to 5K/reel.	Chen S	2025-06-30

DISCLAIMER

- Curve guarantee in the specification. The curve of test items with electric parameter is used as quality guarantee. The curve of test items without electric parameter is used as reference only.
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